A 4e-noise 2/3-inch global shutter 1920x1080P120 CMOS-Imager

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Recently 3x2.2Mpixel CMOS imagers are used in 2/3" Broadcast cameras [1,2], they are rolling shutter type. Imagers in broadcast need to be low noise, high speed, high sensitivity, high Qmax and low dark current. The imager presented in this paper can be used in both rolling shutter and global shutter mode. This imager has an adjustable integration time. Global shutter with exposure control is realized with a 5T pixel.
The vertical scanning in 1920(H)x1080(V) is controlled, either internally through a programmable on-chip state machine (Fig 1: FIT+MUX+FVT) mainly for industrial vision, or externally (MUX+FVT) to allow for broadcast camera performance.
Analog double sampling does reduce kTC noise, with 4T-pixels, in rolling shutter mode. In global shutter mode one needs either an intermediate storage node [3,4] for kTC reduction, or external digital double sampling [2] as applied with this imager. The input to digital double sampling (DDS) is at 1920(H)x1080(V) at 120 frames/sec and the kTC-noise reduced output is at 1920(H)x1080(V) at 60 frames/sec. The 4e read-noise is achieved at a moderate gain of 2x. It allows for a large pixel output swing in highlights, and low noise in black, simultaneously, as needed in broadcast. Normally low noise numbers require a high analog gain [3, 4] reducing the maximum output swing that can be reached.
To reduce image artifacts [5] at highlights each column has a NMOS transistor, with an adjustable gate voltage. It reduces the voltage swing at the input of the analog gain stages and the input of the ADC, preventing overload.
A single LVDS-lane supports a data-rate of up to 1.782Gbps, there are 16 lanes enabling a total of 28.5Gbps.

Fig 1: The imager is fabricated in 0.18um 1P4M technology, with lightshield, and can support 1920(H)x1080(V) up to 240 frames/sec, which is 120frames/sec after DDS . The maximum frame rate is reached with a Sys_clock of 148MHz which aggregates to an equivalent pixelclock of 4x148=592MHz.
The 5T-pixels, figure 2, are placed in an orthogonal lattice. To prevent skew related problems the pixel array is driven from one side.
The imager has a horizontal timing generator (HTIME) and supports region-of-interest readout (ROI). The ROI window width is programmable in 66 blocks of 32 Columns and the rows can be chosen arbitrary.
The vertical scanning of the Image array can be controlled with a build-in token generator (FIT+MUX+FVT) and for demanding applications all vertical scanning tokens can be generated externally and applied to the shiftregisters through the multiplexer (MUX+FVT).
To support high frame rates the odd columns are readout at the bottom side of the pixel array and the even columns at the top, simultaneously.
After sampling at the column capacitor the signal is multiplexed onto one of the 16 switch-capacitor-amplifiers (sca). There are 4x16 switch-capacitor-amplifiers and the output of each set of 16-sca's is routed through an analog multiplexer to one of the ADC inputs. There are 4 ADCs and each one of them is connected to a 4-lane LVDS transmission.
The odd and even rows of the imager array can be addressed independently. The same holds for the odd and even columns. Reading the odd-rows and odd-columns on the bottom side and the even-rows and even-columns at the top side, the pixels are read in zig-zag (quincunx) fashion at 1920x1080Q480 which is 1920x1080Q240 after DDS, doubling the frame rate, without the need for a rhombic shaped pixel [6].

Fig 2 Shows a 5T-pixel with limiter transistor. Each column has a transistor, T_Limiter, that limits the negative going signal excursions through an adjustable voltage at the gate (V_Col_Lim). The source of T_Limiter is connected to the column and the drain to VDD_PIX=3.3V. When the column voltage drops below the gate voltage minus the threshold, transistor T_Limiter takes over. The limiter prevents the current-source at the column to go from saturation into linear region and for the switched-capacitor-amplifiers to go in overload condition. An overload condition often generates an image artifact know as LF-streaking (smearing [5]). The images show the difference with and without the limiter operation.

Fig 3 shows an open eye diagram of an LVDS lane at 1.782Gbps. The imager has 4 ADCs and each ADC has an LVDS-block with 4 lanes. The supported data rate of the 4x4 lanes is 28.5Gbps.

Fig 4 shows a dark current histogram of the Floating Diffusion at 37C, 61C and 77C. The median value for the floating diffusion dark-current is 114e/sec at 37C, 282e/sec at 61C and 720e/sec at 77C, a doubling of the dark-current of about 11C. The dark-current of the photo-diode doubles approximately with 6C: 2.5e/sec at 37C, 38e/sec at 61C and 230e/sec at 77C. The dark current values could be reached through the use of a pinned photo-diode and a pinned-surface underneath the transfer gate and global shutter gate.
A low dark-current is important because the charge is stored at the floating diffusion and the shot noise of the dark-current contributes to the read-noise too.

Fig 5 depicts the scanning in an orthogonal lattice and a zig-zag (quincunx) lattice.

Fig 6: Shows an image taken at 1ms integration time in 1920x1080p60 mode after DDS. The ventilator has no rolling shutter distortion, only motion blur.

The chip specification, measured at 1920x1080p60 after DDS (imager running at 1920x1080p120), is summarized in Table 1. The pixel fill factor without ulens is 44%, Global shutter efficiency is 99.95%, and the conversion gain 95µV/e. The read-noise after DDS is 4e at 27C with an analog gain of 2x. Power dissipation for the imager running at 1920x1080p120 is 1.1W. The size of the active image array is 10.34mmx5.5mm. Chip size is 203mm^2, mounted in a customer defined ceramic package µPGA-185.

References

[1] L. Kozlowski et al, "A Progressive 1920x1080 Imaging System-on-Chip for HDTV Cameras", *ISSCC Dig. Tech. Papers, pp. 358 - 359, Feb 2005*.

[2] P. Centen et.al, *A 2/3-inch CMOS Image Sensor for HDTV Applications with Multiple High DR Modes and Flexible Scanning*, ISSCC Dig. Tech. Papers pp 512-513, Feb 2007.

[3] M. Sakakibara et al, *An 83dB-Dynamic-Range Single-Exposure Global-Shutter CMOS Imager Sensor with in-pixel Dual Storage*. ISSCC Dig. Tech. Papers, pp. 380 - 381, Feb 2012

[4] J. Solhusvik et al, "A 1.2MP 1/3-inch Global shutter CMOS Image Sensor with Pixel-Wise Automatic Gain Selection", International Image Sensor Workshop, Japan, Paper 53, 2011.

[5] M. Purcell et. al, *"Image Artifacts Caused by Pixel Bias Cells in CMOS Imagers targeted for mobile applications"*, International Image Sensor Workshop, Norway, Invited Paper 73, 2009.

[6] T. Toyama et al, *"A 17.7Mpixel 120fps CMOS Image Sensor with 34.8Gb/s Readout*". ISSCC Dig. Tech. Papers, pp. 420 - 421, Feb 2011

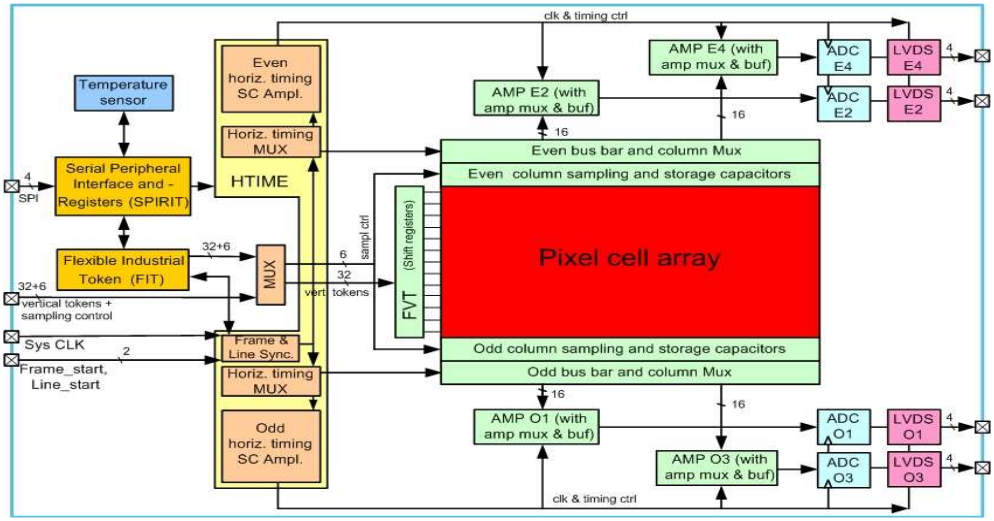


Figure 1: Block diagram of the imager.

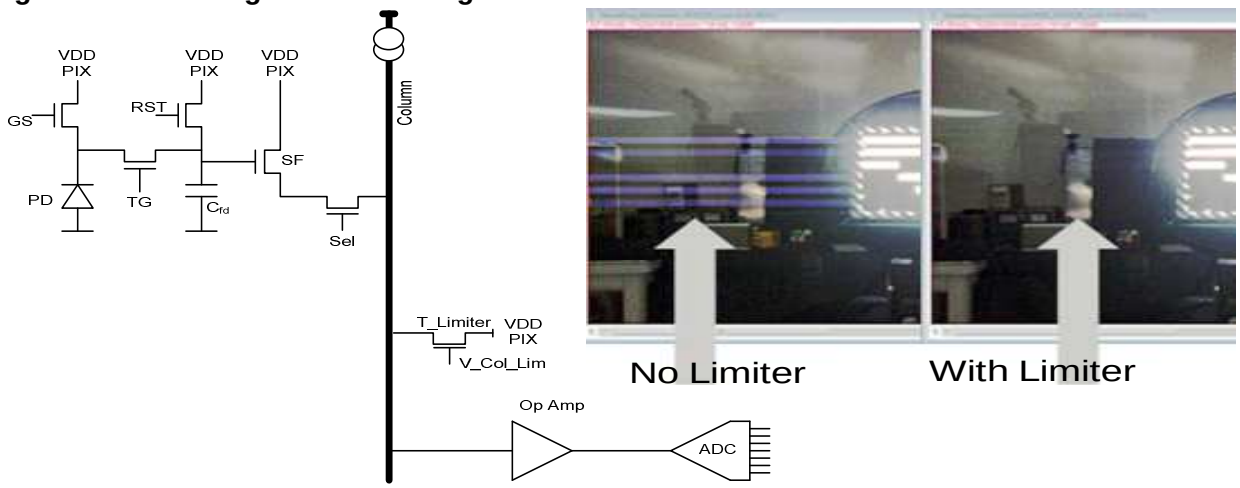


Figure 2: 5T-pixel, with limiter transistor, T_Limiter, at the column to reduce streaking.

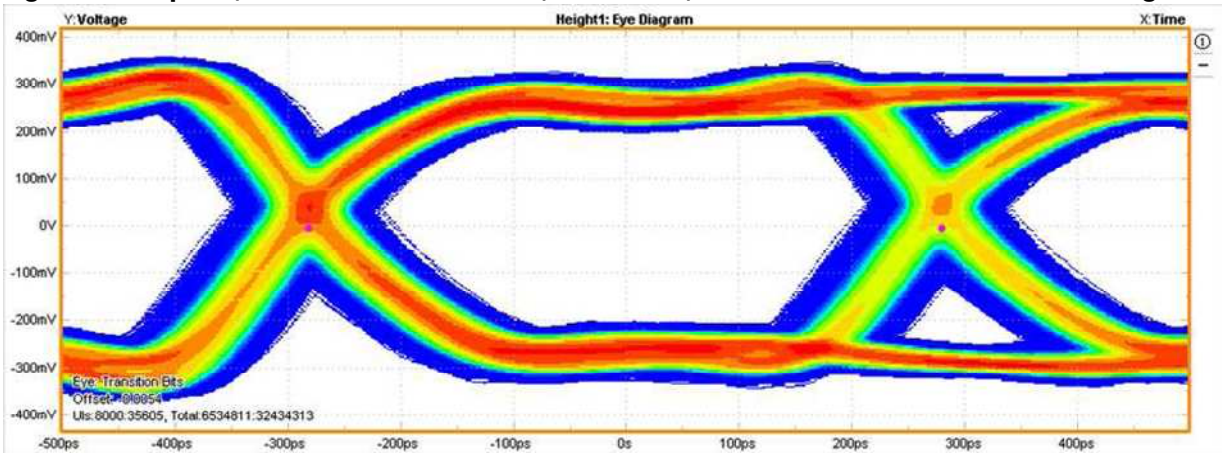
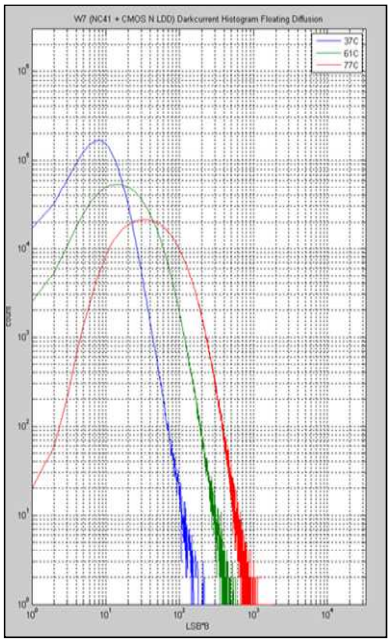


Figure 3: Eye diagram of an LVDS lane at 1.782Gbps



Process	CMOS 0.18 µm 1P4M With light shiield
Supply Voltages	3.3V and 1.8V
Chip Size	203 mm²
Number of light sensitive pixels and overscan pixels	1920+148(H) x 1080+20(V)
Pixel size	5 µm x 5 µm
Transistors per pixel	5T
Pixel Fill Factor	44 % w/o micro-lens
Global shutter efficiency	99.95%
Analog to Digital Conversion LVDS	4 ADCs 4*4 lanes
Max data rate per LVDS lane	1.782 Gbps/lane
Max frame rate	120 frames/sec after DDS rectangular 240 frames/sec after DDS quincunx
PRNU	<1%
Conversion gain FD	95µV/e
Idark FD @ 61C	282 e/sec; 0.18nA/cm^2
Idark PD@ 61C	30 e/sec; 19pA/cm^2
Read Noise@27C	4 e at gain=2x
Sensitivity in Green (495nm – 573nm)	2170 el/lux-sec/um^2
Qmax	>15 kel
Power Dissipation	1.6W @120 frames/sec, DDS 1.1W @ 60 frames/sec, DDS

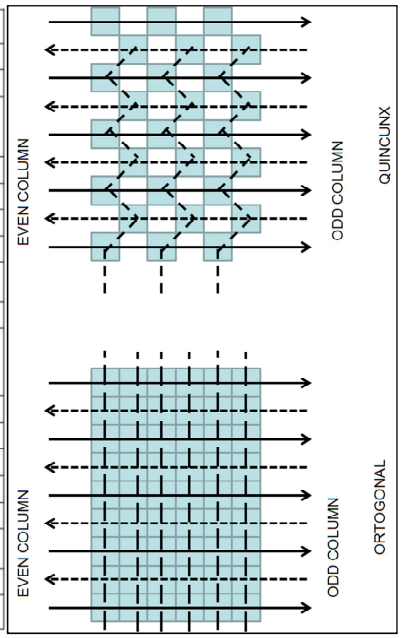


Figure 4 (left): Histogram of the floating diffusion dark current at 37C, 61C and 77C
Table 1 (middle): Device summary.
Figure 5 (right): Orthogonal and zig-zag (quincunx) sample lattice

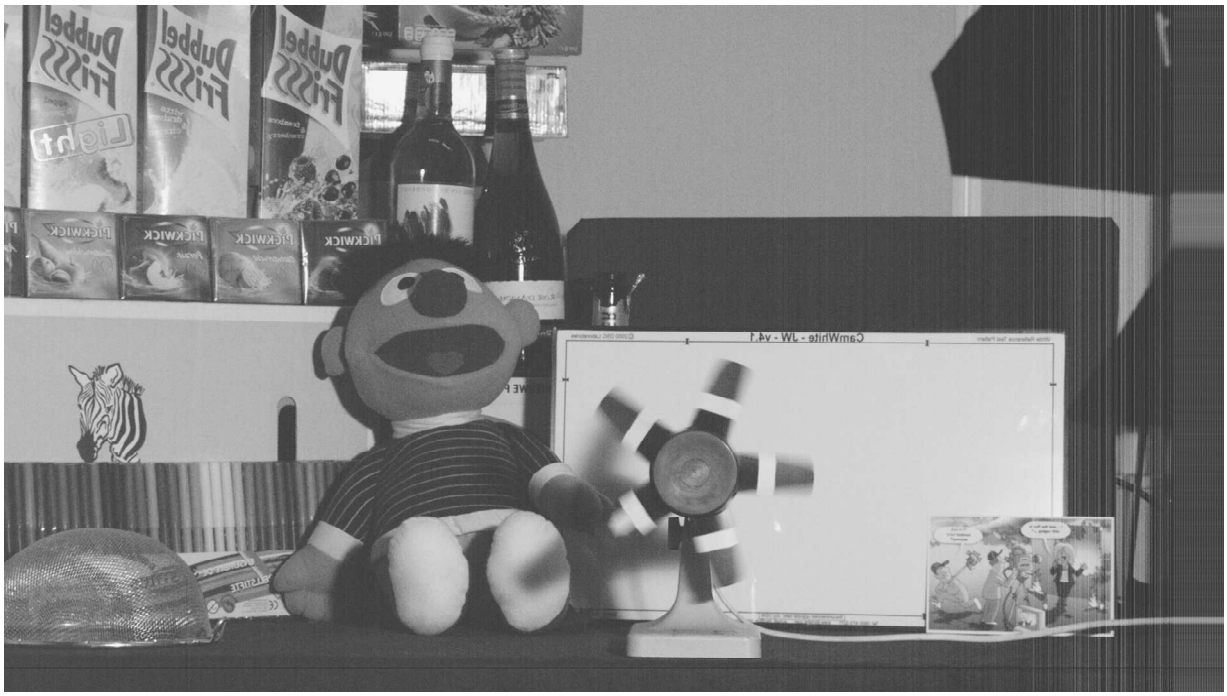


Figure 6: Image after DDS at 1920x1080p60 in global shutter mode at 1ms integration time.