CCD On-Chip Amplifiers: Noise Performance versus MOS Transistor Dimensions

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Abstract—**The effect of change in the channel width, the channel length, and the bias current of detection-node MOS transistors in CCD on-chip amplifiers is studied. A novel approach to noise optimization is shown, and criteria for choosing the optimum gate dimensions are established both in theory and practice. A new parameter, the noise electron density (in square electrons per hertz), is found to be a more suitable parameter for characterizing noise performance. It will be shown that, in a well designed CCD on-chip amplifier, the noise electron density is solely the product of the equivalent gate noise of the detection-node MOS transistor and the total capacitance C_t of the detection node. The noise performance is very insensitive to change in the channel width of a factor of two of the optimum value, but it is sensitive to a change in channel length and bias current. The optimum is valid for every type of signal processing. It is also shown that the bandwidth is smallest during the time the reset FET is in the off-state and that noise increases in this state. The fall time of the sensor signal, during charge sensing, is therefore larger than the rise time during reset, when the charge is drained off. The capacitive feedback, in the reset FET off-state, between the gate and source of the detection-node MOS transistor causes this effect.**

I. Introduction

THIS paper's objective is to establish both in theory and practice the optimum and critical parameters of the detection-node MOS transistor (e.g., the first source follower), namely, the bandwidth, the channel width, the channel length, the bias current, the total capacitance, and the noise electron density.

The main purpose of the on-chip amplifier in a CCD sensor is the conversion of a charge packet into voltage or current. The reset drain naturally is a current output but in general is not used as such. Besides the conversion into a voltage signal or a current signal, the on-chip amplifier must exhibit good noise performance and be capable of driving a load fast enough.

The most popular way of detecting the charge of the CCD channel is to use a floating diffusion [1], [2], which together with the input of the on-chip amplifier is the detection node. The change in the detection-node voltage, caused by the charge, is sensed by the on-chip amplifier.

In order to achieve a large bandwidth, one often encounters a two-stage source follower amplifier; a typical structure is shown in Fig. 1. The first stage consists of a source follower (M_1) and a current sink (M_c) for biasing. Both determine the noise performance. The second stage (M_2) drives the load. For HDTV sensors as many as four stages could be needed.

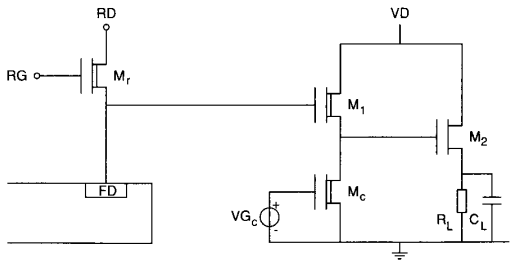

Fig. 1. A typical on-chip amplifier for CCD sensors, with a floating diffusion detection node. From left to right: the reset FET (M_r) is connected to the floating diffusion (FD) and the gate of the first source follower (M_1). With the reset gate (RG) the reset FET can be switched in the on-state and the off-state. In the on-state, FD is reset at the reset drain (RD) level. In the off-state the floating diffusion is floating. In the source of follower M_1, a current sink (M_c) is included. The bias current through M_1 and M_c is controlled with the gate-to-source voltage VG_c. The second source follower (M_2) is driving the load consisting of R_L and C_L.

The reset FET (M_r) is connected to the detection node and consists of the floating diffusion (*FD*) and the gate of M_1. In the on-state it resets the detection node to a reference voltage (*RD*), and in the off-state the floating diffusion can receive the next charge packet. The voltage source between the gate and source (VG_c) of the current sink determines the bias current of the first stage and can be used as a signal injection point to measure the ratio between the total capacitance and the effective sense capacitance (Θ_n) and the bandwidth in the off-state.

In the design of a high-speed amplifier the first stage in part determines the bandwidth, due to the fact that the bandwidth decreases when the reset FET is switched off. The decrease is controlled with the ratio between the total capacitance of the detection-node C_t and the actual sense capacitance C_{fd}. A small part of (C_{fd}) consists of the floating diffusion capacitance. A major part is caused by stray and wiring capacitance and the capacitance of the first MOS transistor. Currently, much attention is devoted to the design of low-capacitance detection nodes, and scaling rules become important. Enlarging a structure on silicon not only enlarges the active MOS transistor capacitances but also the wiring and stray capacitance. It will be shown that the noise performance is proportional to the

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total capacitance C_t of the detection node and the equivalent gate noise voltages of the first MOS transistor.

The designer of a signal processor generally uses the spectral density to determine the optimum processing. In the case of a CCD sensor where the electrons are the signal, it is most natural to use the noise electron density as the equivalent of the spectral density. The noise electron density (in square electrons per hertz) for that matter is the quotient of a spectral density in square volts per hertz divided by the sensitivity (in microvolts per electron) squared.

In contrast to earlier reports about noise optimization in the literature [3], [4] the subject in this paper is approached in quite a different way: the noise optimization is not based on minimizing the noise electrons but on minimizing the noise electron density. It will be shown that the optimum is valid for every type of signal processing (after the CCD).

The reset noise is not taken into consideration because signal processors that are currently available, such as correlated double sampling, suppress the reset noise sufficiently [2], [4]–[8]. In a well designed on-chip amplifier the noise contribution of the first stage exceeds that of the second stage; therefore, the main attention will be devoted to the first stage.

In Section II, the first stage will be analyzed. First, the charge dumping on and the resetting of the floating diffusion will be discussed and the time response calculated just as the 3-dB bandwidth in the reset FET on-state. Finally, the noise is given in a static approach for the on- and off-states. In Section III, the concept of noise electron density is introduced together with a general expression valid for every type of capacitive detection node, both destructive and nondestructive [1], [2], [9]–[12] in which the noise of the detection-node MOS transistor is dominant. In Section IV, a model for noise optimization is presented based on the concept of noise electron density. The optimum dimensions and bias current of the detection-node MOS transistor and current sink are derived in the case of thermal noise. In Section V, experimental verification of the model is presented.

II. The First Stage

A. A Source Follower with Current Sink

A small-signal equivalent diagram of the first stage consisting of a source follower (M_1) and a current sink (M_c) is shown in Fig. 2. The capacitance between the gate and ground (C_1) is made up of the floating diffusion (*FD*), the drain underdiffusion ($C_{gd,u}$), and some stray and wiring capacitance. The capacitance between the gate and the source (C_2) of M_1 consists of the source underdiffusion ($C_{gs,u}$), the active channel capacitance, and stray and wiring capacitance. In the biasing point, the following small-signal parameters are defined. The transconductance of M_1 is g_1, the output resistance R_0 (including the output, resistance of M_1 and M_c), and the capacitive load C_0

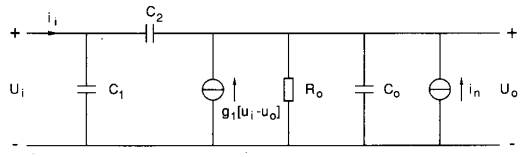

Fig. 2. The small-signal equivalent diagram of the first stage of the on-chip amplifier. C_1 consists of all the capacitances between the gate and ground of M_1, and C_2 consists of all the capacitances between the gate and source of M_1. The transconductance of the source follower M_1 is g_1, the resistive load of M_1 is R_0, and the capacitive load, including the input capacitance of the second MOS transistor, is C_0. The current source i_n represents the noise of both follower M_1 and sink M_c. U_0 is the output voltage at the source of M_1, and U_i is the input voltage. The current i_i is the detection-node current.

(which also includes the input capacitance of the second stage). The current noise source (i_n) represents the noise of both follower M_1 and sink M_c.

Finally, i_i is the current flowing into the detection node. In the reset FET off-state the current i_i is the time derivative of the charge dumped onto the detection node. The reset FET is omitted in the diagram.

When the reset FET is switched from the on- to the off-state, reset noise [1], [2] is generated. Its spectrum depends on the clock frequency and duty cycle of the pulses applied to the reset FET gate (*RG*).

B. Analysis of the Reset FET On- and Off-State

There exists an asymmetry between the reset FET on-state and off-state. In the on-state the detection node is almost short circuited for ac. In the off-state the detection-node is floating and is rather high ohmic for ac; from this moment on, an effective feedback exists from the source to the gate of follower M_1, due to C_2, which forms a capacitive divider with C_1.

In the frequency domain the node equations written in matrix form are

$$\begin{bmatrix} i_i(f) \\ i_n(f) \end{bmatrix} = \begin{bmatrix} j\omega(C_1 + C_2) & -j\omega C_2 \\ -(j\omega C_2 + g_1) & \dfrac{1}{R_0} + g_1 + j\omega(C_0 + C_2) \end{bmatrix} \cdot \begin{bmatrix} U_i(f) \\ U_0(f) \end{bmatrix}. \quad (1)$$

For simplicity's sake, the capacitive load (C_0) is assumed to be much larger than the gate-to-source capacitance of M_1 ($C_0 >> C_2$). The 3-dB bandwidth (F_3) caused by the load capacitance is assumed to be well below the transit frequency ($F_T = g_1/(2\pi C_2)$) of the detection-node MOS transistor (typically 500 MHz–1 GHz).

1) Charge Packet Handling: The Rise Time and Fall Time: In the off-state, charge is dumped onto the floating diffusion. The frequency response of the first stage is calculated by solving the matrix equation (1). By definition, the input current is the time derivative of the charge. After Fourier transformation the relation between input current i_i and the charge packet $Q(f)$ is

$$i_i(f) = j\omega Q(f) \quad (2)$$

putting $i_n(f) = 0$, the response at the source (U_0) becomes

$$U_0(f) = \frac{A_{10}}{1 + j\omega\tau\theta_n} \cdot \frac{Q(f)}{C_{fd}} \tag{3}$$

with the following definitions:

DC gain:

$$A_{10} = \frac{g_1 R_0}{1 + g_1 R_0}. \tag{4}$$

Time constant of the output:

$$\tau = \frac{C_0}{g_1} A_{10}. \tag{5}$$

Effective sense capacitance:

$$C_{fd} = C_1 + (1 - A_{10})\, C_2. \tag{6}$$

The sensitivity of the detection node is determined by the capacitance between the gate and the source of the first MOS transistor (C_2), by the capacitance between the gate and the remainder of the sensor (C_1), and by the voltage gain of the first MOS transistor (A_{10}). Due to the gain (A_{10}) from the gate to the source of follower M_1, only part of the capacitance between those terminals C_2 is "felt."

The total physical capacitance connected to the gate of M_1

$$C_t = C_1 + C_2 \tag{7}$$

and the ratio between the total capacitance C_t and the effective sense capacitance C_{fd} called the sensitivity improvement factor (Θ_n), which is always larger than one in the case of a source follower

$$\theta_n = \frac{C_t}{C_{fd}}. \tag{8}$$

The charge packet in a CCD sensor consists of electrons. Assume that one charge packet with a charge $(-q \cdot N)$ is dumped on the floating diffusion at $t = 0$. In the time domain, this is written as

$$-qN\delta(t) \tag{9}$$

which Fourier transforms to

$$Q(f) = -qN \tag{10}$$

in the frequency domain.

The time response is calculated with the inverse Fourier transformation of (3) with substitution of (10). Introducing the sensitivity as

$$S = A_{10} \frac{q}{C_{fd}} \tag{11}$$

the time response is

$$u_0(t) = V_0 - SN[1 - e^{-t/\tau\theta_n}], \qquad t \geq 0. \tag{12}$$

At $t = 0$, the output voltage has the reference value V_0, and the stationary value ($t = \infty$) is $U_0 = V_0 - S \cdot N$. The output swing due to a charge packet of N electrons is $S \cdot N$. The fall time (12) of the sensor output signal is $\tau\Theta_n$.

Before commenting on the fall time, we first calculate the time response for draining off the charge in the reset FET on-state. In the on-state, the charge dumped in the off-state at the floating diffusion is drained to the reset-drain terminal (*RD*). The equation for the on-state, in the frequency domain, is arrived at by solving (1) with $i_n(f) = 0$

$$U_0(f) = \frac{A_{10}}{1 + j\omega\tau} U_i(f). \tag{13}$$

Assume that at $t = 0$ the output voltage has reached its stationary value V_0 and for $t > 0$ the reset FET is switched on, clamping the floating diffusion at *RD* potential. The response in the time domain is

$$u_0(t) = V_0 - SNe^{-t/\tau}, \qquad t \geq 0. \tag{14}$$

The fall time (12), $\tau\Theta_n$, is increased with a factor $\Theta_n = C_t/C_{fd}$ as compared to the rise time (14), τ.

2) The Bandwidth in the On-State: The on-state is often used to apply a signal at the reset drain in order to measure the bandwidth and the dc gain of the on-chip amplifier. This state is also frequently used to measure the noise performance of the on-chip amplifier. Unfortunately, the results will be far too optimistic as compared with the actual situation when charge is dumped on the floating diffusion in the off-state, as will be shown.

The transfer function (U_0/U_i) in the reset FET on-state is given by the second row of the matrix equation, and with $C_0 >> C_2$ is the same as (13). The 3-dB bandwidth in the on-state is

$$F_3(\text{on}) = \frac{1}{2\pi\tau}. \tag{15}$$

3) The Noise Voltage in the Reset FET On-State and in the Off-State: Only the effect of a noise current i_n at M_1 is considered. The noise current i_n develops a voltage swing at the source of M_1, with the substitution of an equivalent noise voltage $e_n = i_n/g_1$. Equation (1) must now be solved with $C_0 >> C_2$ and due to the fact that the reset FET in the on-state represents a short circuit $U_i = 0$. The solution can be written as

$$U_0(f) = \frac{A_{10}}{1 + j\omega\tau} e_n \tag{16}$$

and in the reset FET off-state ($i_i = 0$)

$$U_0(f) = \frac{A_{10}}{1 + j\omega\tau\theta_n} \theta_n e_n. \tag{17}$$

Comparing (16) with (17), it is noted that the noise of the first stage increases with the factor Θ_n and that at the same time the bandwidth is decreased with that same factor. The 3-dB bandwidth in the reset FET off-state

$$F_3(\text{off}) = \frac{1}{2\pi\tau\theta_n} \tag{18}$$

is smaller than in the on-state (15). This asymmetry between the off-state (12) and the on-state (14) was already noticed for the charge handling. This is a well-known result from feedback theory, which states that, for a given system, the gain-bandwidth product is (almost) a constant. These same conclusions apply for the situation in which the gate of the current source VG_c is used to inject a signal. In this way one can accurately measure Θ_n.

C. The Noise of the Source Follower and the Current Sink

The current sink M_c contributes to the noise of the first stage

$$i_n^2 = i_{n1}^2 + i_{nc}^2. \tag{19}$$

Using the definition of the equivalent noise voltage for M_1

$$e_{n1} = \frac{i_{n1}}{g_1}, \quad \frac{\mathrm{V}}{\sqrt{\mathrm{Hz}}} \tag{20}$$

and M_c

$$e_{nc} = \frac{i_{nc}}{g_c}, \quad \frac{\mathrm{V}}{\sqrt{\mathrm{Hz}}} \tag{21}$$

one gets for the total equivalent noise voltage e_n

$$e_n^2 = e_{n1}^2 + \left[\frac{g_c}{g_1}\right]^2 e_{nc}^2, \quad \frac{\mathrm{V}^2}{\mathrm{Hz}}. \tag{22}$$

The ratio g_c/g_1 is the voltage gain of the cascode section M_c and M_1. It is trivial but very important to note that this gain must be small.

III. The Noise Electron Density

A. Noise Electrons versus NED

In CCD's, it is a common practice to express the noise performance as the number of equivalent noise electrons. This figure of merit is determined by the square root of the product of a noise level (spectral density) and an equivalent noise bandwidth. A low figure can be obtained in two ways: a low-noise level and a small equivalent noise bandwidth. In optimizing for noise performance, it is better to separate the two effects and use as a figure of merit the noise electron density. The equivalent noise bandwidth is determined by signal processing, and the noise electron density is determined by the sensor. Together with the cross-over frequency between the $1/f$ noise and the thermal noise (f_c) of the on-chip amplifier, the noise performance is fully and unequivocally determined. In the case of the equivalent number of noise electrons, one always has the problem of how to incorporate the contribution of the $1/f$ noise.

One usually expresses the noise level as an equivalent noise voltage in volts per the square root of hertz or noise current in amperes per square root of hertz. These units squared are called the voltage spectral density (given as square volts per hertz) and the current spectral density (given as square amperes per hertz). In the case of the sensor with its electrons (charge) as the signal, it is more appropriate to express the noise in square electrons per hertz for which we propose the name noise electron density (NED). This value can be given in two states: the reset FET on-state and the off-state. Of course the value in the off-state must be given because this is the state in which charge is dumped on the detection node. This is also the state in which the signal processor suppresses reset noise and $1/f$ noise [2], [4]–[8] and amplifies the charge signal.

Using (3) for the sensitivity with the charge (Q) equal to the unit charge $Q = q$ and using (8) and (17), the expression for the NED becomes

$$\mathrm{NED}(f) = \left[\frac{e_n(f)\,C_t}{q}\right]^2 \left(\frac{\mathrm{e}^2}{\mathrm{Hz}}\right). \tag{23}$$

This equation also includes $1/f$ noise since it is valid for every frequency.

Already, one can state that it is a necessity for a noise optimum that the MOS transistor channel-independent capacitances contained in C_t are as small as possible. Furthermore, the gain A_{10} of the first stage does not appear in the formula. Neither does the sense capacitance C_{fd}.

Expression (23) can be generalized to be true for every capacitive detection node (Fig. 3(a)) when the following conditions are fulfilled:

- the noise of the detection-node MOS-transistor is dominant, and
- the only high ohmic node in the charge-detection system during charge sensing is the gate of the detection-node MOS transistor.

Now one can show that the NED is proportional to the sum of all the capacitances connected to this gate multiplied by the intrinsic noise properties of the detection-node MOS transistor (e_n).

Proof: The current noise source (i_n) across the MOS transistor source and drain can be shifted towards the gate by the use of $e_n = i_n/g$, (Fig. 3(b)). After application of the Blakesly transformation:

> "a single voltage source in one branch may be shifted through a node by removing the voltage source from that branch and adding it to every other branch connected to that node" (Fig. 4(a)) "a single current source between two nodes can be split up into two current sources in series and the middle point can be connected to an arbitrary third node" (Fig. 4(b))

and the Norton–Thevenin transformation to change a voltage source into an equivalent current source or visa versa (Fig. 4(c)) the detection-node is represented Fig. 3(c) with its capacitances (C_i) and two injecting current sources, one of which is the charge ($j\omega Q$) and the other the noise current ($j\omega C_t e_n$). With the total capacitance as

$$C_t = \sum_{1}^{N} C_i. \tag{24}$$

No attention has been paid to the effect of the noise currents at the other points of the respective capacitors C_i

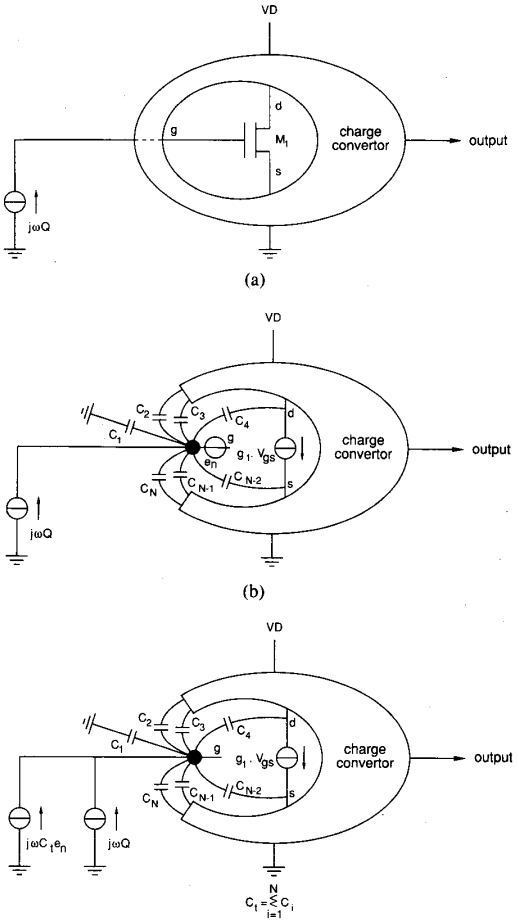

Fig. 3. (a) A general scheme of a capacitive detection-node with an MOS transistor as the first stage in the charge convertor (M_1). The charge dumped on the detection node is represented by a current source $j\omega Q$. (b) As in (a), but now the small-signal equivalent diagram is drawn with the noise current i_n of the detection-node MOS transistor transformed into an equivalent noise voltage e_n. The capacitances C_1, C_2 up to C_N are the capacitances that are physically connected to the detection node. The transconductance of the MOS transistor M_1 is g_1. (c) As in (b) with the equivalent noise voltage (e_n) of the detection-node MOS transistor transformed using the rules for shifting a voltage source through a node, a transformation of a voltage source into a current source, and splitting a current source into two equal ones. After neglecting the contribution of the current sources at the low ohmic part of the system, the result is a current noise source at the detection node itself.

because of the realistic condition that the detection node was the only high ohmic node in the system in the reset FET off-state.

B. After Signal Processing

Depending on the camera system one wants to minimize the noise in a bandwidth (B) of 5 MHz (PAL), 4.2 MHz (NTSC), or 30 MHz (HDTV). In general, the on-chip amplifier noise spectrum contains a $1/f$ portion. Many CCD signal processors suppress the $1/f$ noise and the reset noise [2], [4]–[8]. One can show [7] that the

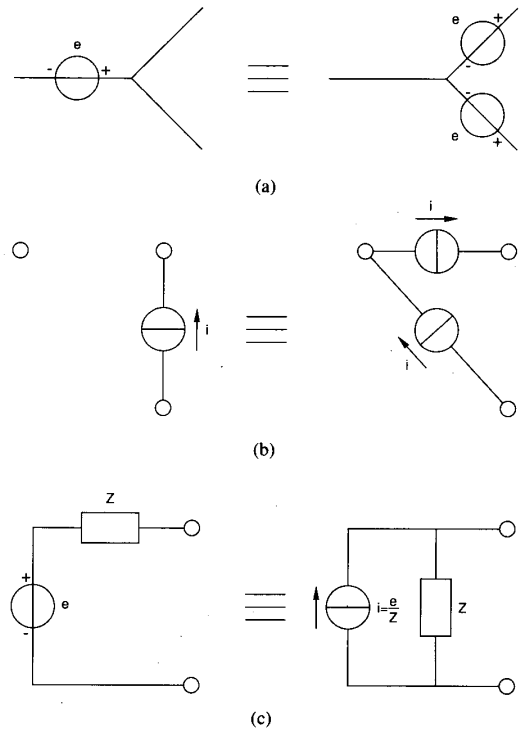

Fig. 4. (a) Represents the Blakesly transformation of a single voltage source (e) in one branch through a node into the remaining branches. (b) Is the transformation of a current source (i) between two nodes into two current sources between those two nodes and a third one. (c) Is the Norton–Thevenin transformation of a voltage source into an equivalent current source.

number of noise electrons squared due to thermal noise after signal processing in a bandwidth (B) can be written as the product of bandwidth B, the NED before signal processing, and a noise increasing factor $\langle M \rangle$ due to signal processing

$$N_{\text{amp}}^2 = \langle M \rangle \, B \, \text{NED} \, e^2 \tag{25}$$

where B is the bandwidth in which one measures the noise. $\langle M \rangle$ is a multiplication factor[1] that gives the average increase of noise due to processing when a white noise source is used as input to the signal processing; it is a figure of merit for the ideal signal processor.

$\langle M \rangle$ and B are signal processing dependent and the NED depends on the CCD-sensor only. Therefore, in the

[1]With a rather straightforward calculation one can show that, for the correlated double sampler and the correlated clamp sample, the factor $\langle M \rangle$ equals

$$\langle M \rangle = 4 \frac{B_n}{f_s} \int_0^B \left[\frac{\sin\left(\pi \frac{f}{f_s}\right)}{\pi \frac{f}{f_s}} \right]^2 \frac{1}{B} \, df$$

with B_n the noise bandwidth at the sampler and/or clamp, f_s the clock, frequency at the output of the signal processing, and B the bandwidth in which one measures the noise after signal processing.

case of thermal noise only, any noise minimum stays a minimum no matter what signal processor one uses.

In the case where $1/f$ noise is also present, one can show [7] that (25) is still valid except that the NED must now be given at a frequency near the clock frequency with which the reset FET is switched. The reason for this is rather simple: A minimum condition for suppressing $1/f$ noise and reset noise is that the signal processing has a gain equal to zero for $f = 0$ Hz. The first gain peak of the processing must be near the reset FET clock frequency and there the noise will also peak.

IV. Model for Noise Optimization

A. The Noise Electron Density for Thermal Noise

The model outlined in this paper is also valid for floating-gate detection nodes, and even for every type of capacitive detection node. The number of noise electrons after signal processing is only determined by the thermal noise when the turnover frequency between the $1/f$ noise and the thermal noise of the on-chip amplifier is far below the reset FET clock frequency [4], [7]. This is the case with the measurements outlined in Section V.

In Section III, a general expression for the NED was derived in (23). In the case of thermal noise only, one arrives at a simple expression. Using the simple saturated MOS transistor model for the equivalent noise voltage [13] of the detection-node MOS transistor M_1 and the current sink MOS transistor M_c

$$e_{n1}^2 = 4kT\frac{\alpha}{g_1}\ \frac{\mathrm{V}^2}{\mathrm{Hz}} \tag{26}$$

and

$$e_{nc}^2 = 4kT\frac{\alpha}{g_c}\ \frac{\mathrm{V}^2}{\mathrm{Hz}} \tag{27}$$

The constant α is $2/3$ for the ideal MOS transistor without back-bias effect. With back-bias effect [13]–[15], it becomes $2/3 \cdot (1 + g_b/g)$ with g the transconductance from the gate to the source and g_b the back-bias transconductance from the back bias to the source. At short channel lengths the electron temperature [16] increases and

$$\alpha = \frac{2}{3}\left(1 + \frac{g_b}{g}\right)\frac{T_e}{T} \tag{28}$$

with T_e the electron temperature and T the lattice temperature.

Substituting the equivalent noise voltage of follower M_1 (26) and sink M_c (27) into (22) and equating (23), one arrives at the expression for the NED as

$$\mathrm{NED} = \alpha\frac{4kT}{g_1}\left[1 + \frac{g_c}{g_1}\right]\left[\frac{C_1 + C_2}{q}\right]^2. \tag{29}$$

The two terms between brackets represent the relative contribution to the thermal noise by the current sink (M_c): 1: g_c/g_1.

B. The Total Capacitance C_t

Changing the dimensions of a detection-node MOS transistor at the silicon level changes the total capacitance C_t. The components of C_t are proportional to:

- the area ($W_1 \cdot L_1$) such as the MOS transistor channel capacitance (C_{gs}),
- the length L_1 in the overlap of the gate on the inactive area ($C_{g,0}$),
- the width W_1 in the underdiffusion of the drain and source regions ($C_{gs,u} + C_{gd,u}$), and
- a fixed part such as wiring, stray capacitances, and floating diffusion (C_{fixed}).

$$\begin{aligned} C_t &= C_{gs} + C_{g,0} + C_{gs,u} + C_{gd,u} + C_{\mathrm{fixed}} \\ &= AW_1L_1 + BL_1 + CW_1 + D. \end{aligned} \tag{30}$$

A, B, C, and D are proportional constants that are determined by layout. With measurements on actual structures, one can fit these parameters. Based on this formula, one can define a typical channel width W_T to be used in normalizing the channel width W_1 for optimization.

$$W_T = \frac{BL_1 + D}{AL_1 + C}. \tag{31}$$

The capacitances C_1 and C_2 can be determined from direct measurements of Θ_n and A_{10} and C_{fd}

$$C_2 = \frac{C_{fd}}{A_{10}}(\theta_n - 1) \tag{32}$$

and

$$C_1 = \frac{C_{fd}}{A_{10}}[\theta_n(A_{10} - 1) + 1]. \tag{33}$$

After calculation of these values, it is possible to locate and reduce parasitic capacitances; how this was done in our sensors to improve the noise performance is beyond the scope of this paper.

C. Minimum NED

Due to the fact that a current sink is used to bias the source follower M_1, the optimization must be carried out with respect to the bias current I (not the gate-to-source voltage) and two parameters that determine the dimensions of the follower such as the channel width W_1 and the channel length L_1. The transconductance in the simple saturated MOS transistor model [17] is written as

$$\begin{aligned} g_1 &= \sqrt{2K\frac{W_1}{L_1}I} \\ g_c &= \sqrt{2K\frac{W_c}{L_c}I}. \end{aligned} \tag{34}$$

Substituting C_t (30) and g_1 (34) in (29), the expression for the NED becomes

$$\text{NED} = \alpha \frac{4kT}{\sqrt{2KI}}\left[1 + \sqrt{\frac{W_c}{L_c}\frac{L_1}{W_1}}\right] \cdot \sqrt{\frac{L_1}{W_1}} \cdot \left[\frac{AW_1L_1 + BL_1 + CW_1 + D}{q}\right]^2. \quad (35)$$

The trivial part of the optimum is given by the smallest channel length L_1 (process determined) and highest bias current I. The optimum value of the channel width W_1 is determined by the value of W_1 for which the first derivative of NED with respect to W_1 is zero.

After using W_T as a normalizing width ($w := W_1/W_T$), the optimum width is the solution of

$$0 = \sqrt{w}(3w - 1) + 2\beta(w - 1). \quad (36)$$

The parameter β accounts for the influence of the current sink MOS transistor

$$\beta = \sqrt{\frac{W_c}{L_c}\frac{L_1}{W_T}} \quad (37)$$

with W_c and L_c, the channel width and length of M_c, respectively.

Two special cases can be considered: $\beta = 0$ and $\beta = \infty$. The first case has as optimum channel width $W_1 = W_T/3$ and the second $W_1 = W_T$. One can show by inspection of (36) that the optimum channel width will always be between $W_T/3$ and W_T. The solution for the optimal channel width as a function of β (36) is given in Fig. 5 (W/W_T branch). The optimum width is always between $W_1 = W_T/3$ (noise of follower $M_1 >>$ noise of sink M_c) and $W_1 = W_T$ (noise of $M_1 <<$ noise of M_c) depending on the contribution of M_c to the noise. Fig. 5 also shows the relative contribution (29) of M_c's noise (g_c/g_1 branch) with respect to the noise of the source follower M_1. At a value of $\beta = 1$, the current sink M_c contributes even more than the source follower M_1 itself. Of course, one should try to keep β as small as possible.

Optimum Signal-to-Noise Ratio: For a good signal-to-noise ratio, the NED must be as small as possible:

1) Make all the detection-node MOS-transistor (M_1) independent capacitances as small as possible.
2) Make the length (L_1) of the MOS transistor channel as small as is practically possible.
3) Determine the constants in the scaling rules for C_t, such as A, B, C, D.
4) Give the channel width (W_1) of the MOS transistor its optimum value (Fig. 5). The W_1/L_1 of the first MOS transistor is now determined.
5) Make the bias current (I) as large as is practically possible and g_c/g_1 as small as possible by choosing the gate-to-source bias voltage of the current sink as high as possible.

The practical length is determined by hot-electron effects and channel shortening. At short channel lengths, the gain (A_{10}) decreases and the contribution of other stages to the noise may not be neglected any more.

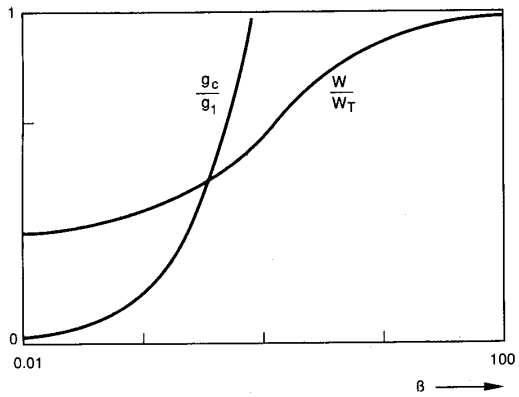

Fig. 5. The optimum channel width W of the detection-node MOS transistor as a function of the parameter that describes the effect of the current sink $\beta = \sqrt{W_cL_1/(L_cW_T)}$. The optimum width W is normalized with the typical width $w = W/W_T$. Also shown is the relative noise contribution of the current sink (g_c/g_1) as a function of (β) when the detection-node MOS transistor has its optimum channel width.

In the case where the parasitics such as under-diffusion capacitance and overlap capacitance are negligible a simple interpretation of the optimum is possible. The optimum value of the gate-to-source capacitance of the detection-node MOS transistor will always be between

$$\tfrac{1}{3} C_{\text{fixed}} \le C_{gs} \le C_{\text{fixed}}. \quad (38)$$

The left-hand side is an equality value when the noise contribution of the current source is negligible and the right-hand side when the noise of the current source dominates. Recalling that for a saturated MOS transistor the gate to source capacitance equals

$$C_{gs} = \tfrac{2}{3} C_g$$

the inequality can be written as

$$\tfrac{1}{2} C_{\text{fixed}} \le C_g \le \tfrac{3}{2} C_{\text{fixed}}.$$

In a well designed on-chip amplifier, the noise contribution of the current source will be small, and the optimal gate capacitance is therefore about half the value of all the fixed capacitance.

D. Sensitivity of the Optimum with Respect to the Parameters W, L, and I

Evaluating (35) as a function of W_1/W_{opt}, one can show that by choosing the actual width W_1 between $W_{\text{opt}}/2$ and $2 \cdot W_{\text{opt}}$ the noise performance only deteriorates by 0.5 dB, see Fig. 6. The thermal noise decreases with increasing current I. The largest gain can be made by externally increasing the gate-to-source voltage of the current MOS transistor M_c. The other possibility is to increase the W_c/L_c of the current MOS transistor and to connect the gate to the source (bulk MOS transistor). Now an increase of bias current I results in a decrease of noise, but this effect is counteracted due to the increased thermal noise contribution of the current sink. Finally, the thermal noise

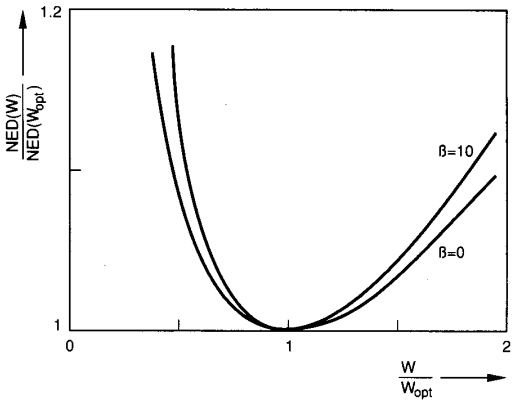

Fig. 6. The predicted relative change in noise electron density as a function of deviations from the optimum value of the channel width W_1 of the detection-node MOS transistor. The horizontal axis is W_1/W_{opt}. In both cases the relative change in the noise electron density is very small even when the change in channel width is large.

decreases with decreasing channel length L_1 for as long as the hot-electron region is not reached and the channel length shortening is not too large.

V. Experimental Verification of the Model

In a test chip a number of two-stage on-chip amplifiers (Fig. 1) with a CCD delay line were designed with different W/L for the detection-node MOS transistor M_1. The gate of the current sink was separately connected to a bonding pad to control the bias current (I) of the current MOS transistor M_c and source follower M_1. It also serves as a signal injection point to measure the bandwidth in the reset FET on- and off-states and the sensitivity improvement factor Θ_n.

A. The Total Capacitance of the Detection-Node

The total capacitance is given by rearranging (8) $C_t = \Theta_n C_{fd}$. To obtain the total capacitance C_t the following measurements had to be performed:

1) The sensitivity (in microvolts per electron) and the gain from floating diffusion to the output was measured, and from this the effective sense capacitance C_{fd} was calculated.
2) The sensitivity improvement factor Θ_n was measured in two steps using the gate of the current sink M_c as an injection point and measuring the gain from the gate to the output in the reset FET off-state and in the on-state and dividing them: Θ_n = Gain(off)/Gain(on) (see (16) and (17)).

Fig. 7 shows the effective sense capacitance C_{fd} as a function of the effective channel width W_1 and the channel length L_1 as a parameter. The total capacitance C_t as a function of these same parameters is shown in Fig. 8. Recalling (30) and attributing the different coefficients to the layout, one gets

$$C_t = A \cdot W_1 \cdot L_1 + B \cdot L_1 + C \cdot W_1 + D$$

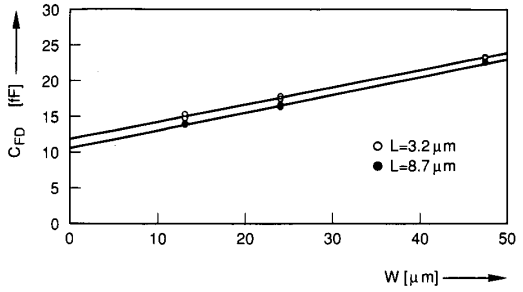

Fig. 7. The effective sensing capacitance C_{fd} at the input of the detection node as a function of channel width W_1 and with the channel length L_1 as a parameter. The solid lines are fits, and the dots are measurements.

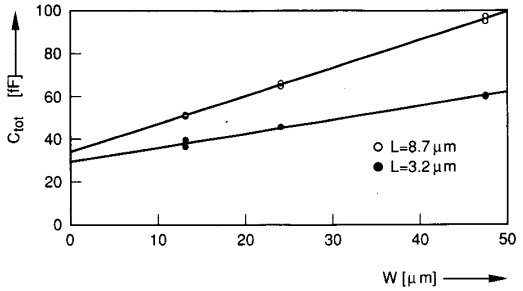

Fig. 8. The total capacitance of the detection node C_t as a function of channel width W_1 and with the channel length L_1 as a parameter. The solid lines are fits, and the dots are measurements.

where A is mainly determined by the MOS-transistor channel capacitance, B is the overlap with the inactive area, C is the underdiffusion of both the drain and source regions, and D is the wiring, stray, and floating diffusion.

The straight lines fit into the measurements in Fig. 8:

$$C_t = 0.12 \cdot W_1 \cdot L_1 + 0.58 \cdot L_1 + 0.27 \cdot W_1 + 29 \text{ [fF]}$$

with L_1 and W_1 in micrometers. The scaling rules for the capacitance can be measured quite well with this procedure, by calculating C_1 and C_2 separately with (32) and (33). It was possible to establish parasitic capacitances that could be reduced considerably, giving improved noise performance.

B. The 3-dB Bandwidth

Measurement on an older type of on-chip amplifier is shown in Fig. 9. It reveals the decreased bandwidth and the increased voltage gain between the gate of the current sink (M_c) and the output in the off-state. In a sensor, the bandwidth in the reset FET on-state can easily be measured by injecting a small signal at the reset drain. In the off-state one could use the output gate (the blocking barrier gate between the horizontal CCD channel and the detection node) to capacitively inject a signal at the input of the on-chip amplifier.

The decrease of bandwidth as predicted in (15) and (18) will in practice be smaller than Θ_n due to the fact that the second stage also limits the bandwidth. The sensitivity

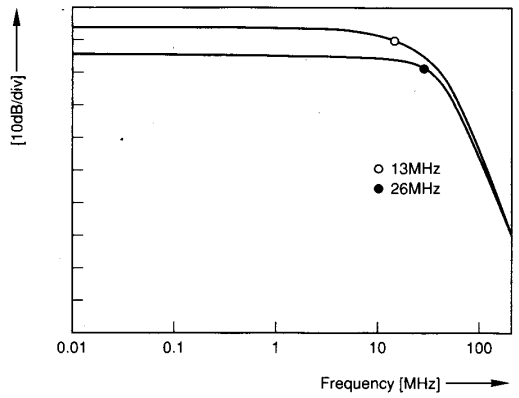

Fig. 9. Measurement of the gain from the gate of the current sink MOS transistor to the output of the on-chip amplifier as a function of frequency. The top curve is measured in the reset FET off-state and the bottom in the reset FET on-state. The markers show the 3-dB cutoff frequencies.

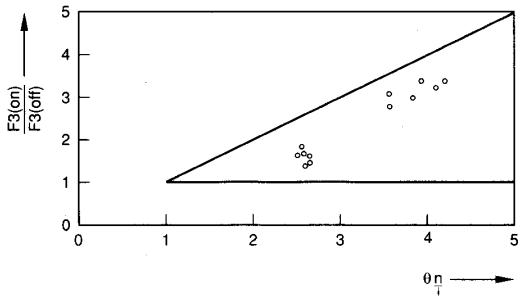

Fig. 10. The ratio between the 3-dB frequencies in the on-state and the off-state $F_3(\text{on})/F_3(\text{off})$ as a function of Θ_n. The solid lines show the upper bound (Θ_n) and the lower bound (1) as a function of Θ_n. The dots represent the measurements.

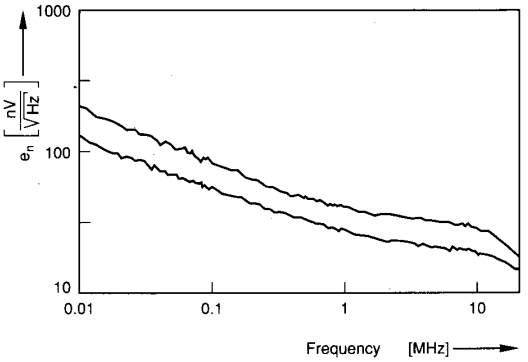

Fig. 11. A noise measurement on a test module. The upper trace is the noise in the reset FET off-state, and the lower trace in the on-state.

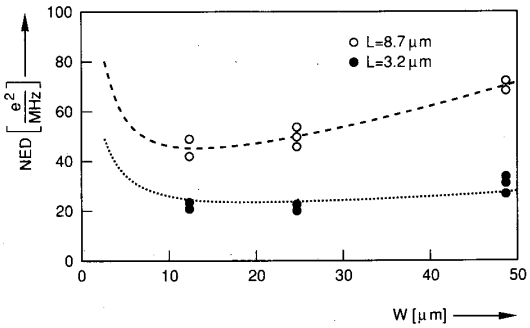

Fig. 12. The noise electron density of the thermal noise as a function of the channel width W_1 and with the channel length L_1 as a parameter. The bias current is 100 μA. The dots are measurements, and the dotted lines are predictions.

improvement factor Θ_n is therefore an upper bound for the decrease in bandwidth. A lower bound for the ratio $F_3(\text{on})/F_3(\text{off})$ is one.

In Fig. 10 the ratio $F_3(\text{on})/F_3(\text{off})$ is plotted against Θ_n. As is clear, the ratio stays within the upper bound given by Θ_n and the lower bound of one.

C. The Optimum Value of the Channel Width

In Fig. 11 a typical static noise measurement is shown of the $1/f$ and thermal noise in the reset FET on-state and in the reset FET off-state. Notice the increase of the noise in the reset FET off-state. The increase is less than Θ_n due to the fact that the thermal noise of the reset FET channel increases the thermal noise in the reset FET on-state.

From the measured scaling rules for the total capacitance C_t, the typical width W_T given in (31) and the normalized parameter β for the current sink M_c in (37) are calculated.

At $L_1 = 3.2$ μm, $W_T = 47$ μm, $\beta = 0.17$, and $w = 0.43$.
At $L_1 = 8.7$ μm, $W_T = 26$ μm, $\beta = 0.38$, and $w = 0.51$.

The solution of (36) for the optimum width w is also given in the last column. The corresponding respective optimum channel widths are $W_1 = 20$ and 13 μm.

A smaller optimum when the channel length is larger seems odd. But in fact, the optimum states that the gate capacitance of the detection-node MOS transistor should equal a given value (see (38)). Therefore, an increasing channel length results in a smaller optimum channel width.

In Fig. 12 the NED is shown as a function of the channel width W_1 and with the length L_1 as a parameter. The weak dependence on the width, as predicted, is clearly seen. This is similar to the smaller optimum width at a longer channel length.

In Fig. 13 the NED as a function of bias current I for one of the samples is given and the $1/\sqrt{I}$ dependence is obvious, as predicted.

After a correlated clamp sample, the noise electrons were measured in a bandwidth of 5 − 0.2 = 4.8 MHz. The on-chip amplifiers are used at a clock frequency of 5 MHz. The $1/f$ corner frequency is well below this frequency ($F_c < 0.5$ MHz) and the thermal noise approach is valid. The noise electrons as a function of channel width W_1 with the gate-to-source bias voltage of the current sink (VG_c) as a parameter are shown in Fig. 14. (Changing the gate-to-source voltage VG_c changes the bias current I.)

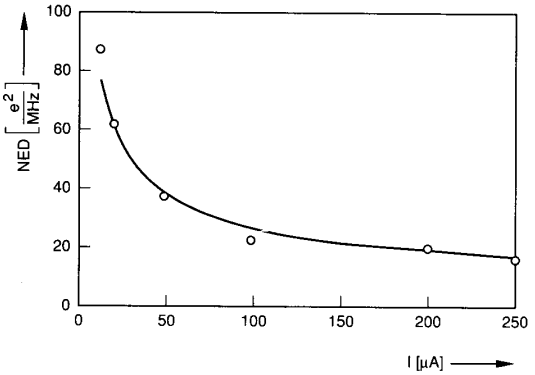

Fig. 13. The noise electron density of the thermal noise as a function of the bias current I of one of the test modules. The dots represent measurements, and the solid line is the predicted bias current dependence $(1/\sqrt{I})$.

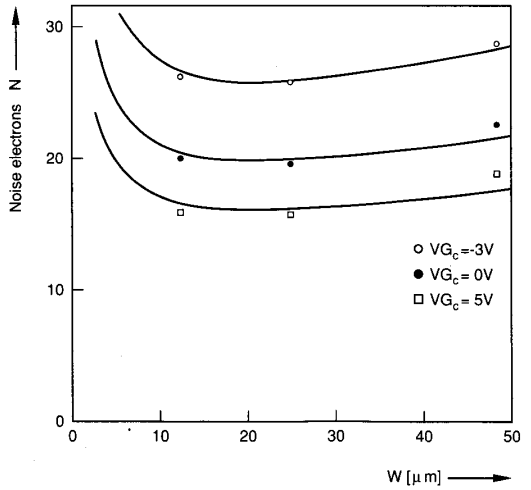

Fig. 14. The noise electrons after correlated clamp sample as a function of source follower channel width W_1 and with the gate-to-source voltage of the current sink as parameter. The channel length is $L_1 = 3.2$ μm. The dots are measurements, and the solid lines are predictions.

After signal processing, the same soft minimum behavior is seen as in the NED (see Fig. 12).

VI. Conclusion

With the aid of specially designed test modules it is possible to measure the scaling rules for the total capacitance C_t and, together with C_{fd} and A_{10}, determine the capacitance between the gate and ground C_1 and the capacitance between the gate and the source of the detection-node MOS transistor C_2. These are used to locate possible parts in the design that could be improved. The underdiffusion can be determined just as the MOS transistor channel capacitance and overlap capacitance.

It is proven that the thermal noise optimum has a weak dependence on the channel width of the source follower MOS transistor near its optimum value. It depends more strongly on bias current and channel length. With the simple MOS transistor model, it was possible to calculate the optimum value of the channel width, which is in good agreement with measurements.

It was shown that the bandwidth in reset FET off-state is smaller than in the on-state. The fall time of the sensor output signal is shown to be larger than the rise time. Furthermore, the value for the sensor bandwidth has been shown to be too optimistic when measured by injection at the reset drain. The same applies to the noise in this state. The sensitivity improvement factor $\Theta_n = C_t/C_{fd}$ is of extreme importance.

It is also proven that the NED (in square electrons per hertz) is a natural noise quantity for charge detection nodes, as in CCD sensors. The NED depends on the product of the equivalent gate noise voltage of the first stage and the total capacitance connected to the floating diffusion, and this is valid for every type of capacitive charge detection node. The NED and therefore the noise electrons do not depend on the gain of the on-chip amplifier and are not directly related to the sensitivity. Therefore, the design strategy should be to minimize the total capacitance even when the improvement in sensitivity is low. Attention must be focused on the total capacitance. The noise optimum for the on-chip amplifier does not depend on the signal processor that is used. The sensor determines the NED, and the signal processor determines the equivalent noise bandwidth, which determines processing performance.

With respect to the noise optimum, the channel length of the detection-node MOS transistor should be as small and the bias current should be as large as is practically possible. The channel width should be given its optimal value as established by the scaling rules. The current sink should have a small W/L, and its gate-to-source bias voltage must be as large as possible.

Acknowledgment

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