The Double-Sided Floating-Surface Detector: An Enhanced Charge-Detection Architecture for CCD Image Sensors

Edwin Roks, *Member, IEEE*, Peter G. M. Centen, Jan T. Bosiers, *Member, IEEE*, and Wim F. Huinink

***Abstract*—A new high speed, low noise, nondestructive charge detector, called the Double-Sided Floating-Surface Detector (DSFSD), which is fabricated in a standard CCD image sensor process, is reported. This detector can be integrated in CCD image sensors and is capable of detecting large charge packets at very low noise levels. Typical values are 5–8 noise electrons (within a bandwidth of 5 MHz) for a charge packet size of 100 000 to 250 000 electrons. The detector is used as the first MOS transistor in a three-stage source-follower configuration with a bandwidth of 150 MHz. The performance of both the traditional Floating-Surface Detector and Double-Sided Floating-Surface Detector (DSFSD) are calculated using a new, simple, model. This model is experimentally verified.**

I. Introduction

TWO sources of noise determine the noise performance of present CCD imagers: fixed-pattern noise (FPN) caused by dark-current nonuniformities, and thermal noise from the output amplifier. The first one is tackled by almost completely eliminating the surface dark current of the imager [1]. For this reason more attention has to be paid to the output amplifier because its noise contribution dominates, even at higher temperatures. The traditional floating-diffusion amplifier (FDA) [2] has a relatively high noise level because its sensing capacitance cannot be made sufficiently small. In order to be able to exploit the performance of CCD's, some alternative output structures with lower noise have been presented. The floating-surface detector (FSD) [3]–[5] is one of the most promising structures. Top-views of both the usual FDA and the FSD are shown in Fig. 1. The difference between these two detectors is that in the second a pMOS transistor is fully integrated with the CCD channel, which results in a much smaller sensing capacitance. In the FSD, the floating diffusion is replaced by an n channel with a much lower dope. Because of this lower doping, the channel can be depleted (reset) completely and therefore the structure produces no kTC noise. The original implementation of this detector suffered several drawbacks. First, the detector was only capable of handling a maximum of approximately 10 000 electrons per charge packet, which is not sufficient for image sensor applications.

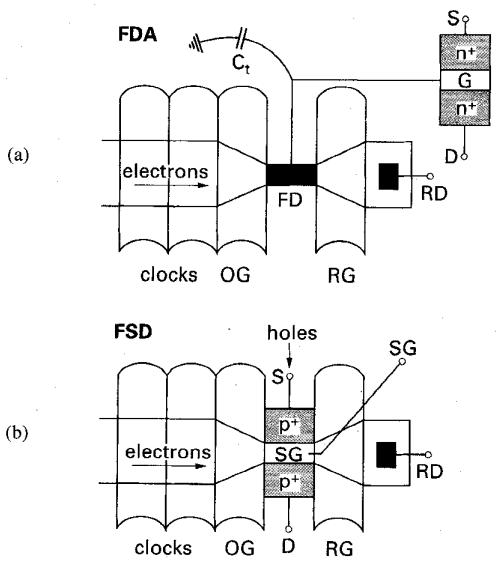


Fig. 1. Top views of (a) the floating-diffusion amplifier (FDA) and (b) the floating-surface detector (FSD).

Second, it was optimized for high responsivity instead of high dynamic range, using a thick gate oxide (1 μm) and consequently high gate voltages. Finally, it was difficult to simultaneously confine both type of carriers (electrons and holes) of the CCD and the detection channel because the CCD channel stop was of the same type as the source and drain of the FSD [5]. In this work we will show that these problems can be solved by introducing the Double-Sided Floating-Surface Detector (DSFSD).

The following chapters (II, III and IV) discuss the Floating-Surface Detector including a simple model to describe it's performance. This model is also valid for the Double-Sided Floating-Surface Detector (DSFSD) which will be discussed in the remaining chapters.

II. Operation of the Floating-Surface Detector

Fig. 2(a) shows a top view of the floating-surface detector. The sensing gate (SG) is set to be strongly negative to ensure that inversion takes place at the MOS transistor surface. In spite of the negative gate voltage an additional deep n implant ($DN2$) under the SG forms a potential well for

Manuscript received November 1, 1995; revised May 23, 1996. The review of this paper was arranged by Editor W. F. Kosonocky.

The authors are with Philips Imaging Technology, Philips Research Laboratories Eindhoven, 5656 AA Eindhoven, The Netherlands.

Publisher Item Identifier S 0018-9383(96)06459-3.

electrons. Electrons can be clocked along the CCD channel (Fig. 2(b)); when they appear under the SG they modulate the free hole concentration and hence the channel conductance of the transistor (Fig. 2(c)). After detection the electrons are reset by a normal reset MOS transistor. The reset pulse completely depletes the sensing channel, which means that the detector produces no reset noise (kTC noise) from the CCD channel. The floating-surface detector is usually operated in source-follower configuration using a constant current source. The effect of modulation of the free-hole concentration by an electron charge packet can be understood from a simple one-dimensional model (the source-drain voltage is taken to be zero). In this model (Fig. 3 is showing the potential profile under the SG) the device is considered to be completely depleted except for a signal charge packet and a surface hole concentration. N_D, N_A, N_{Ds} are the ion concentrations per cm^2 of the n channel ($DN + DN2$), the p well (DP) and the n substrate, respectively, σ_n is the electron charge and σ_p the surface hole charge, both per cm^2. l is the depletion depth underneath the packet and d the depth of the center of gravity of the charge packet. Using Gauss' law,

$$\epsilon_{\text{ox}} E_{\text{ox}} = \sigma_p - \sigma_n + q(N_D - N_A + N_{Ds}) \tag{1}$$

where E_{ox} is the electrical field in the oxide. From (1) it follows that, because the surface potential is constant and therefore the field E_{ox} is constant, a change in σ_n will result in a change in σ_p and qN_{Ds}. This coupling between σ_n and σ_p can be described by

$$\Delta\sigma_p = \Delta\sigma_n\left(1 - \frac{1}{1 + \frac{l}{d}}\right) \approx \Delta\sigma_n\left(1 - \frac{d}{l}\right) \quad \text{for } l \gg d \tag{2}$$

and is better when d/l is small.

III. Performance of the Floating-Surface Detector

In a proper amplifier design, the first stage of the amplifier is dominant with respect to noise and responsivity. Therefore, in this section only the performance of the single-stage floating-surface detector, operated as a source follower with an ideal current-source load, will be taken into account. As the surface channel of the floating-surface detector is modulated by a charge packet, which can be regarded as a sort of buried gate, the traditional MOS transistor equations cannot be applied directly. Therefore a new model is required for the further calculation of noise and responsivity. In this section this model will be derived and the responsivity will be calculated. From the model a small-signal diagram will be generated, which will be used for noise calculations.

As $n = N_d$ in the charge packet, with n being the electron concentration and N_d the ion concentration both per cm^3, the charge-packet voltage (buried-gate voltage) is determined by the electron Fermi potential

$$V_p = \phi_n + \frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right) = \phi_n + \text{const.} \tag{3}$$

From Fig. 4, presenting the capacitance model of the floating-surface detector, it follows that the local charge per area $\sigma(x)$

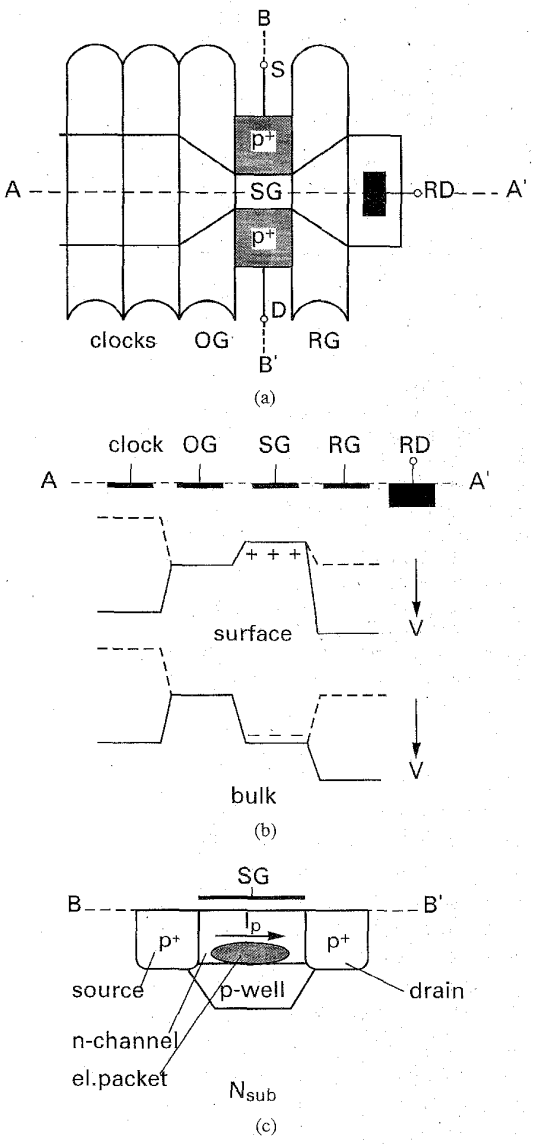


Fig. 2. (a) Top view of a floating-surface detector, (b) cross-section over A-A′, showing both the surface and the channel potentials, (c) cross-section over B-B′ (x direction), showing the p-channel transistor.

(Ccm^{-2}) along the surface hole channel is given by

$$\sigma(x) = C_{\text{pc}_\square}(V(x) - V_p) + C_{\text{gc}_\square}(V(x) - V_g) \tag{4}$$

with $V(x)$ being the local channel potential, V_g the sensing-gate potential, V_s the source potential, V_d the drain potential and V_N the substrate potential. The current in the channel as a function of x is represented by

$$I = \frac{E(x)W d_c}{\rho(x)} = -q\mu_p p\frac{\partial V(x)}{\partial x}W d_c = -\mu_p\sigma(x)W\frac{\partial V(x)}{\partial x}. \tag{5}$$

In this equation W, E, d_c, ρ and μ_p are the width of the transistor channel, the electric-field component in the x direction, the thickness of the channel, the resistivity and the mobility of the surface holes, respectively. Integration over the total

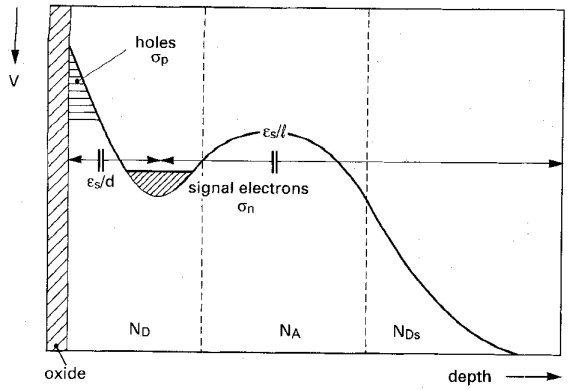


Fig. 3. 1-Dimensional model illustrating the modulation of surface holes by the electron charge packet.

transistor length results in (Appendix A)

$$I = \frac{1}{L}\int_0^L I dx$$
$$= \mu_p \frac{W}{L}\left((C_{\mathrm{pc}_\square} V_{\mathrm{ps}} + C_{\mathrm{gc}_\square} V_{\mathrm{gs}})V_{\mathrm{ds}} - (C_{\mathrm{pc}_\square} + C_{\mathrm{gc}_\square})\frac{V_{\mathrm{ds}}^2}{2}\right) \quad (6)$$
$$= \mu_p \frac{W}{L}\left(\eta V_{\mathrm{ds}} - \xi\frac{V_{\mathrm{ds}}^2}{2}\right) \quad (7)$$

where

$$\eta \equiv C_{\mathrm{pc}_\square} V_{\mathrm{ps}} + C_{\mathrm{gc}_\square} V_{\mathrm{gs}} \text{ and } \xi \equiv C_{\mathrm{pc}_\square} + C_{\mathrm{gc}_\square}$$

In saturation $\sigma = 0$ at pinch off and therefore $V_{\mathrm{ds}}^{\mathrm{sat}} = \eta/\xi$. For I_{sat} it follows that

$$I_{\mathrm{sat}} = \frac{\mu_p}{2}\frac{W}{L}\frac{\eta^2}{\xi}. \quad (8)$$

This is analogous to the normal MOS transistor equation, with the allowance for the back bias effect. g_m and g_p, the transconductance of the sensing gate (SG) and the charge packet to the surface channel, respectively can be derived from I_{sat}. This way the charge packet is treated as a buried gate in the substrate.

$$g_m = \frac{\partial I_{\mathrm{sat}}}{\partial V_{\mathrm{gs}}} = \frac{\mu_p W}{L}\frac{\eta}{\xi}C_{\mathrm{gc}_\square} = C_{\mathrm{gc}_\square}\sqrt{2\frac{\mu_p}{\xi}\frac{W}{L}I_{\mathrm{sat}}} \quad (9)$$

$$g_p = \frac{\partial I_{\mathrm{sat}}}{\partial V_{\mathrm{ps}}} = \frac{\mu_p W}{L}\frac{\eta}{\xi}C_{\mathrm{pc}_\square} = C_{\mathrm{pc}_\square}\sqrt{2\frac{\mu_p}{\xi}\frac{W}{L}I_{\mathrm{sat}}}. \quad (10)$$

If I_{sat} is taken to be constant, because of the source-follower configuration with ideal load, the ratio of ΔV_s and ΔV_p is the DC gain A_0 of the structure. It follows from

$$\Delta I_{\mathrm{sat}} = \frac{\partial I_{\mathrm{sat}}}{\partial V_{\mathrm{ps}}}\Delta V_{\mathrm{ps}} + \frac{\partial I_{\mathrm{sat}}}{\partial V_{\mathrm{gs}}}\Delta V_{\mathrm{gs}} \quad (11)$$
$$= g_p(\Delta V_p - \Delta V_s) - g_m \Delta V_s = 0. \quad (12)$$

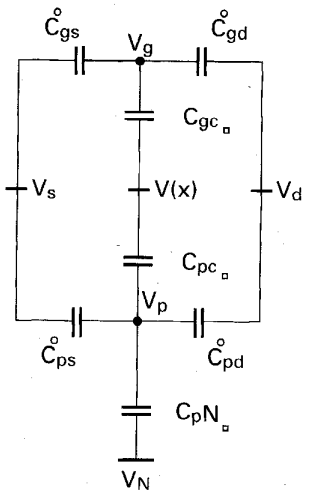


Fig. 4. Capacitance model of the floating-surface detector.

From this it follows that

$$\frac{\Delta V_s}{\Delta V_p} = \frac{g_p}{g_m + g_p} = \frac{C_{\mathrm{pc}_\square}}{C_{\mathrm{pc}_\square} + C_{\mathrm{gc}_\square}} \equiv A_0. \quad (13)$$

To be able to calculate the capacitances in the structure, the total charge Q_c in the surface channel and the total charge Q_p in the charge packet have to be calculated first. The total charge in the surface channel Q_c can be split into two parts: a part compensated by the electron charge packet (Q_{cp}) and a part compensated by the gate (Q_{cg}). When the two parts are added together $-2\eta/3$ is obtained (Appendix B). This is the total charge in the surface channel. The charge in the electron packet, at the node V_p shown in Fig. 4, is given by

$$-qN_{el} = Q_p$$
$$= C_{\mathrm{ps}}^o(V_p - V_s) + C_{\mathrm{pd}}^o(V_p - V_d) + WL$$
$$\times\left(C_{pN_\square}(V_p - V_N) + \frac{C_{\mathrm{pc}_\square}}{L}\int_0^L (V_p - V(x))dx\right) \quad (14)$$

where C_{pd}^o and C_{ps}^o are in this context overlap capacitances. The last term of (14) results in (Appendix B)

$$\frac{C_{\mathrm{pc}_\square}}{L}\int_0^L (V_p - V(x))dx = C_{\mathrm{pc}_\square}\left(V_{\mathrm{ps}} - \frac{\eta}{3\xi}\right). \quad (15)$$

Therefore, with respect to the transistor's source, (14) results in

$$-qN_{el} = Q_p$$
$$= C_{pN}(V_{\mathrm{ps}} - V_{Ns}) + C_{\mathrm{ps}}^o V_{\mathrm{ps}} + C_{\mathrm{pd}}^o(V_{\mathrm{ps}} - V_{\mathrm{ds}})$$
$$+ C_{\mathrm{pc}}V_{\mathrm{ps}} - \frac{1}{3}\left(\frac{C_{\mathrm{pc}}}{C_{\mathrm{pc}} + C_{\mathrm{gc}}}\right)(C_{\mathrm{pc}}V_{\mathrm{ps}} + C_{\mathrm{gc}}V_{\mathrm{gs}}), \quad (16)$$

where

$$C_{..} \equiv WLC_{..\square}.$$

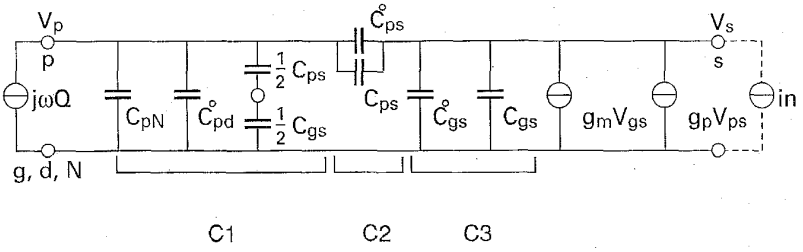


Fig. 5. Small-signal diagram of floating-surface detector.

The responsivity can be calculated directly from this relation. A change in the electron charge results in

$$\begin{aligned} -q\Delta N_{el} = \Delta Q_p &= C_{pN}(\Delta V_{\rm ps} + \Delta V_s) + C^o_{\rm ps}\Delta V_{\rm ps} \\ &+ C^o_{\rm pd}(\Delta V_{\rm ps} + \Delta V_s) + C_{\rm pc}\Delta V_{\rm ps} \\ &- \frac{1}{3}\left(\frac{C_{\rm pc}}{C_{\rm pc}+C_{\rm gc}}\right)(C_{\rm pc}\Delta V_{\rm ps} - C_{\rm gc}\Delta V_s) \quad (17) \end{aligned}$$

$$\Longrightarrow \Delta V_{\rm ps} = -\frac{q\Delta N_{el} + \left(C_{pN} + C^o_{\rm pd} + \frac{C_{\rm pc}C_{\rm gc}}{3(C_{\rm pc}+C_{\rm gc})}\right)\Delta V_s}{C_{pN} + C^o_{\rm ps} + C^o_{\rm pd} + C_{\rm pc} - \frac{C^2_{\rm pc}}{3(C_{\rm pc}+C_{\rm gc})}}. \quad (18)$$

From $\Delta I_{\rm sat} = 0$ it follows that $\Delta\eta = 0$ and

$$\Delta V_{\rm ps} = \Delta V_s \frac{C_{\rm gc}}{C_{\rm pc}}. \quad (19)$$

Combination of (18) and (19) results in the responsivity

$$\begin{aligned} {\rm resp} &= \frac{\Delta V_s}{\Delta N_{el}} \\ &= -\frac{qC_{\rm pc}}{C_{\rm pc}(C_{pN} + C^o_{\rm pd}) + C_{\rm gc}(C_{pN} + C^o_{\rm ps} + C^o_{\rm pd} + C_{\rm pc})}. \end{aligned} \quad (20)$$

A corresponding small-signal diagram is required for further analysis. To this end the capacitances of the channel have to be expressed into capacitances of the source. The total charge at the source can be written as

$$\Delta Q_s = \Delta Q^o_s + \Delta Q_c, \quad (21)$$

where ΔQ^o_s is the variation in charge due to the overlapping of the gate and the source and ΔQ_c is the variation in surface-channel charge. The total gate-to-source capacitance is

$$C_{{\rm gs}_{\rm tot}} \equiv \frac{\partial Q_s}{\partial V_g} = \frac{\partial Q^o_s}{\partial V_g} + \frac{\partial Q_c}{\partial V_g} = C^o_{\rm gs} + \frac{2}{3}C_{\rm gc}, \quad (22)$$

where $C^o_{\rm gs}$ is the gate-source overlap capacitance.

$$C_{\rm gs} \equiv \frac{2}{3}C_{\rm gc}. \quad (23)$$

In an analogous way it follows that

$$C_{{\rm ps}_{\rm tot}} \equiv \frac{\partial Q_s}{\partial V_p} = \frac{\partial Q^o_s}{\partial V_p} + \frac{\partial Q_c}{\partial V_p} = C^o_{\rm ps} + \frac{2}{3}C_{\rm pc} \quad (24)$$

and

$$C_{\rm ps} \equiv \frac{2}{3}C_{\rm pc}. \quad (25)$$

For the capacitance from the packet to the gate it follows from (16) that

$$C_{pg} \equiv \left.\frac{\partial Q_p}{\partial V_g}\right| = \frac{1}{3}\frac{C_{\rm pc}C_{\rm gc}}{C_{\rm pc}+C_{\rm gc}} = \frac{1}{2}\frac{C_{\rm ps}C_{\rm gs}}{C_{\rm ps}+C_{\rm gs}}. \quad (26)$$

These relations result in the small-signal diagram presented in Fig. 5. The responsivity can also be obtained directly from the corresponding small-signal diagram. Substitution of $j\omega Q$ (the Fourier transform of $Qd(t)$ where $Q = -qN_{el}$) for the input current results in the responsivity (see Appendix C)

$${\rm resp} = \frac{-qA_0}{C_1 + C_2(1-A_0)} = \frac{-qA_0}{C_{\rm in}} \quad (27)$$

where

$$C_1 \equiv C_{pN} + C^o_{\rm pd} + \frac{1}{2}\frac{C_{\rm ps}C_{\rm gs}}{C_{\rm ps}+C_{\rm gs}} \text{ and } C_2 \equiv C_{\rm ps} + C^o_{\rm ps}.$$

Using (23) and (25), this equation results in (20). This approach therefore leads to the same result.

When the oxide thickness would be infinite, $C_{\rm gs}$ would be zero and the responsivity would be

$${\rm resp} = -\frac{q}{C_{pN} + C^o_{\rm pd}}. \quad (28)$$

To create a high responsivity, the gate-oxide must therefore be as thick as possible. To ensure a large fringing field and therefore fast transport in the CCD, the potential maximum must be at a depth of approximately 0.3 μm [6]. This results in $C_{\rm gc} \approx C_{\rm pc}$ for an oxide thickness of 0.1 μm and therefore in a DC-gain of 1/2. The responsivity is in this case found to be

$${\rm resp} \approx -\frac{q}{C_{\rm pc}} \quad (29)$$

where C_{pN} and the capacitances due to overlapping are smaller than $C_{\rm pc}$. Compared with (28) this equation gives a more realistic value with respect to imager applications.

For device performance it is essential to look at noise behavior and not just at responsivity. In general the device noise spectrum contains a thermal portion and a $1/f$ portion. The CCD signal processing will in general suppress the $1/f$ noise [2]. Therefore, only the thermal noise contribution is taken into account. To model this, an extra noise source i_n should be added to the small-signal diagram (Fig. 5). The noise voltage at the source, Vs_n, can be calculated as a function of i_n, with V_p floating (see Appendix D). This results in the relation

$$\langle V^2_{S_n}\rangle = \frac{\langle i^2_n\rangle {\rm resp}^2 C^2_t}{q^2 g^2_p} = \frac{\langle i^2_n\rangle}{g^2_p}A^2_0\left(\frac{C_t}{C_{\rm in}}\right)^2. \quad (30)$$

The total performance is now calculated using the *Noise Electron Density* (NED) $[(e^-)^2\ \mathrm{Hz}^{-1}]$ introduced by Centen [2] as an equivalent of the *Voltage Spectral Density* $[V^2\ \mathrm{Hz}^{-1}]$. In the NED the noise voltage is normalized with respect to responsivity. The NED is found to be

$$\mathrm{NED} \equiv \frac{\langle V_{S_n}^2 \rangle}{\mathrm{resp}^2} = \frac{\langle i_n^2 \rangle C_t^2}{g_p^2 q^2}. \tag{31}$$

By integrating the NED over the bandwidth (B) the number of noise electrons squared after signal processing equals

$$N_{\mathrm{noise}}^2 = \langle M \rangle \int_0^B F(\omega)\mathrm{NED}(\omega)d\omega. \tag{32}$$

In this equation $\langle M \rangle$ represents a multiplication factor (figure of merit) that gives the average increase in noise due to processing when a white noise source is the input to the signal processing. When for a single output a traditional correlated double sampler is used, $\langle M \rangle$ equals 4 [2]. In the case of no reset noise, a low-pass filter is enough for good processing and $\langle M \rangle$ equals 2. In this calculation, $\langle M \rangle$ is taken to be 4 for a worst-case scenario. $F(\omega)$ is the processing filter characteristic. It is often taken to be 1, also in a worst-case scenario. The noise of the first stage is determined without an electron charge packet in the channel. It consists of the thermal noise from the sensing gate, the back-bias and the current source. At the source this results in the noise current i_n.

$$\langle i_n^2 \rangle = 4kT\alpha(g'_m + g_b + g_c) \tag{33}$$

where g'_m is the transconductance of the gate without a charge packet in the channel, g_b the transconductance of the back-bias and g_c the transconductance of the current-source load. The constant α is 2/3 for the ideal MOS transistor without back-bias effect [7]. g'_m and g_b are found using the relation for I_{sat} without a charge packet in the channel $(= I'_{\mathrm{sat}})$

$$I'_{\mathrm{sat}} = \frac{\mu_p}{2}\frac{W}{L}\frac{(\eta')^2}{\xi'} \tag{34}$$

where

$$\eta' \equiv C_{Nc_\square} V_{Ns} + C_{\mathrm{gc}_\square} V_{\mathrm{gs}} \quad \text{and} \quad \xi' \equiv C_{Nc_\square} + C_{\mathrm{gc}_\square}$$

analogously to (9) and (10), g'_m and g_b are defined as

$$g'_m = \frac{\partial I'_{\mathrm{sat}}}{\partial V_{\mathrm{gs}}} = \frac{\mu_p W}{L}\frac{\eta'}{\xi'}C_{\mathrm{gc}_\square} = C_{\mathrm{gc}_\square}\sqrt{2\frac{\mu_p}{\xi'}\frac{W}{L}I'_{\mathrm{sat}}} \tag{35}$$

$$g_b = \frac{\partial I'_{\mathrm{sat}}}{\partial V_{Ns}} = \frac{\mu_p W}{L}\frac{\eta'}{\xi'}C_{Nc_\square} = C_{Nc_\square}\sqrt{2\frac{\mu_p}{\xi'}\frac{W}{L}I'_{\mathrm{sat}}}. \tag{36}$$

When $F(\omega)$ is taken to be 1 and $\langle M \rangle = 4$, the number of noise electrons is

$$N_{\mathrm{noise}} = 2\sqrt{B\mathrm{NED}}. \tag{37}$$

In the next section these equations will be used to optimize the floating-surface detector with respect to noise behavior.

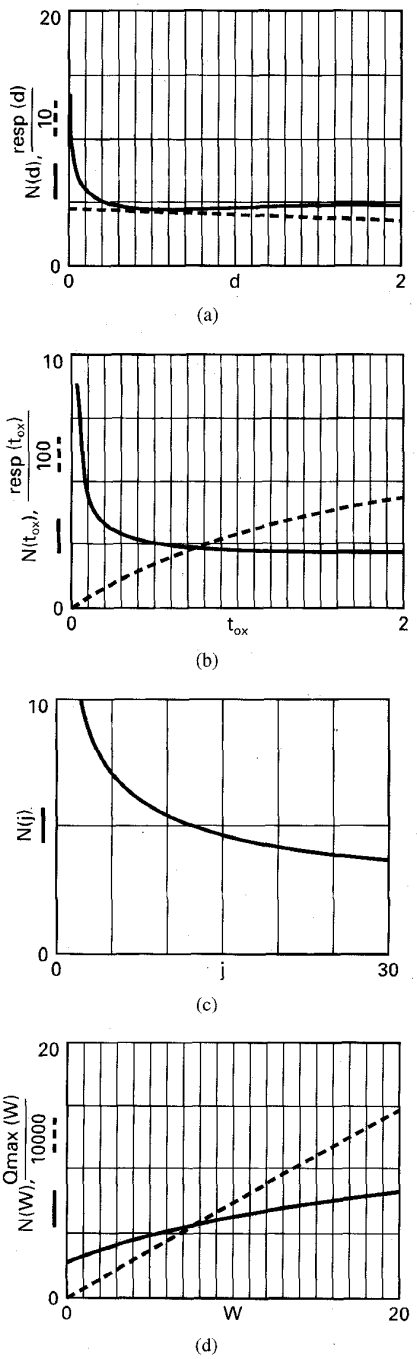


Fig. 6. Simulation of N, responsivity and charge-handling capability vs. charge packet depth (a), oxide thickness (t_{ox}), current density (c), and transistor width (W).

IV. Modeling of the Floating-Surface Detector

A. Performance as a Function of FSD Dimensions

The floating-surface detector was optimized with respect to noise and maximum charge-handling capability using the simple model described in the previous chapter. The parameters varied were: the transistor width (W) of the detector, the oxide thickness (t_{ox}), the depth (d) of the charge packet

TABLE I
RESULTS OF CURRY SIMULATION AND THE ANALYTICAL VALUES

	CURRY simulation	analytical model
DC gain (small packet)	0.33	0.30 (d=0.7 μm)
DC gain (large packet)	0.48	0.38 (d=0.5 μm)
responsivity	32 $\mu V/e^-$	39 $\mu V/e^-$ (d=0.5 μm)
C_{ps}/W	0.51 $fF\mu m^{-1}$	0.51 $fF\mu m^{-1}$ (d=0.5 μm)
C_{gs}/W	0.84 $fF\mu m^{-1}$	0.85 $fF\mu m^{-1}$

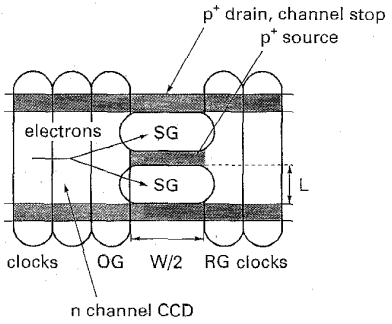


Fig. 7. Top view of Double-Sided Floating-Surface Detector (DSFSD).

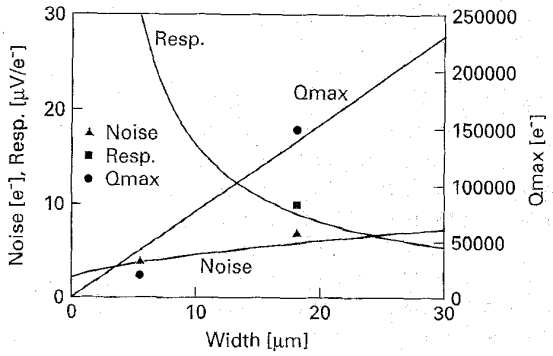


Fig. 8. Number of noise electrons (Noise), charge-handling capability ($Q_{\max}$) and responsivity (resp) versus the transistor width. The filled markers indicate the measurements. The markers at $W = 6$ μm indicate the measurements of the FSD, the markers at $W = 18$ μm indicate the measurements of the DSFSD.

and the hole-current density. The load of the floating-surface detector was characterized by a load with $g_c^{-1} = 200$ kΩ.

The capacitances were estimated using a simple relation for the saturated MOS model

$$C_{pN}(W) = WL\frac{\epsilon_S}{l} \tag{38}$$

$$C_{\rm gs}(W, t_{\rm ox}) = \frac{2}{3}WL\frac{\epsilon_{\rm ox}}{t_{\rm ox}} \tag{39}$$

$$C_{\rm ps}(W, d) = \frac{2}{3}WL\frac{\epsilon_S}{d} \tag{40}$$

$$C_{\rm pd} = 0. \tag{41}$$

In Fig. 6(a) and (b) the noise (solid lines) and responsivity (dotted lines) are given as functions of the packet depth (μm) and the oxide thickness (μm). In the first simulation W/L was 4/3.7, the oxide thickness 0.1 μm and the current density 15 μAμm^{-1}. In the second simulation the packet depth was fixed at 0.5 μm and the oxide thickness was varied from 0 to 2 μm. The noise was corrected for responsivity using the NED. These graphs emphasize that for low-noise operation it is important to store the charge packet at a depth not less than 0.5 μm, which is the normal channel depth used in buried-channel CCD structures. It further shows that oxide-thicknesses of more than 0.5 μm are not needed (the number of noise electrons N is almost stable beyond 0.5). The consequence of this last observation is that low operating voltages can be used, which makes the structure more attractive for applications in CCD cameras.

Because the floating-surface detector was in our application used in a standard CCD process with an oxide thickness of 0.1 μm a "*flat potential plate*" as described by Matsunaga *et al.* [4], in the gate oxide (between the sensing gate and the silicon-oxide interface), was not needed. The described potential pockets do not exist in structures with such gate oxides. In the third calculation (Fig. 6(c) the current density (μAμm^{-1}) was varied. In the last calculation (Fig. 6(d)) the noise and maximum charge-handling capability were plotted against the width (μm) of the FSD. For a charge-handling capability of 150 000 electrons a width of 20 μm is required. According to the noise curve (Fig. 6(d)) this will increase the amount of noise electrons with respect to the $W/L = 4/3.7$ case from 4 to 8 electrons.

B. Device Simulations

A 3D off-state simulator (PADDY) and a 2D on-state simulator (CURRY) were used for the device simulations, to simultaneously model signal electrons in the bulk potential well and a hole current from the p^+ source to the p^+ drain along the Si-SiO$_2$ interface. The 3D simulations were carried out to estimate the maximum charge-handling capability of the detector and to check the different barriers in the device.

The 2D dynamic CURRY simulations were carried out in the lateral direction (in the plane of the source and drain) to determine the different parasitic capacitances and consequently the saturation current, responsivity and gain. Following the previous results, L was taken to be 3.7 μm and the oxide thickness was 0.1 μm. Table I compares the simulation results with the analytical model.

C. Confinement of Electrons and Holes

A difficult problem in designing the floating-surface detector is the required simultaneous confinement of electrons and

TABLE II
COMPARISON BETWEEN THE FDA, FSD, AND DSFSD

	FDA	FSD (t_{ox}=1μm)	DSFSD (t_{ox}=0.1μm)
detection	destructive	non-destructive	non-destructive
max. charge	≈2·10^5 e^-	≈1·10^4 e^-	≈2·10^5 e^-
responsivity	10 $\mu V/e^-$	200 $\mu V/e^-$	10 $\mu V/e^-$
Noise	15 e^-	4 e^-	8 e^-
SG voltage	-	-60 V	-5 V

holes. Several leakage paths may exist in the device: a path under the output gate (OG) and the reset gate (RG), leakage through the p well from the source to the drain when the p well is not completely depleted and leakage from the p^+ source to the p^+ drain along the p^+ channel stop.

The first leakage path is blocked by choosing the appropriate potentials for the output gate and the reset gate (i.e., by keeping the reset gate clock at a small negative value, as shown in Fig. 2(b)). The second path can be blocked by doping the p well only slightly and making the surface potential under the sensing gate (SG) sufficiently low. The third path is our major concern. It can be blocked by making the structure double-sided, as will be explained in the next chapter.

V. THE DOUBLE-SIDED FLOATING-SURFACE DETECTOR (DSFSD)

A. Device Description

Fig. 7 shows a top view of a DSFSD. The sensing gate (SG) is split into two parts and the surface MOS transistor has its source area in the middle of the CCD and its drain area in common with the CCD channel stop. With this layout, the problem of simultaneous confinement of electrons and holes is completely solved. For a good noise performance, the length of the transistor L has to be as small as possible (see Chapter IV). The charge-handling capability is increased by making the transistor wider. Although this larger width (W) increases the total capacitance, it also increases the transconductance and current of the transistor. Therefore the net noise increase is low. The speed of the detector is fast even at higher values of W (e.g., 20 μm) because the transport length is $W/2$.

B. Evaluation

Three test structures have been designed to evaluate the DSFSD concept: two FSD structures $W = 6$ μm, $L = 3.7$ μm, $t_{ox} = 1$ μm and $W = 6$ μm, $L = 3.7$ μm, $t_{ox} = 0.1$ μm, and a DSFSD $W = 18$ μm, $L = 3.7$ μm. All structures are operated as a source-follower, using a (low-capacitance) load resistor of 200 kΩ. The load resistor was made of an n channel in a completely depleted p well at a reverse bias connected to the p well of the CCD and the detector (to drain the holes and make the structure more compact). This resulted in a low capacitance, and therefore in a large bandwidth. A CCD line with 7 stages was coupled to the test structure to inject signal charge. Fig. 8 shows the measurement results of both devices. They fit nicely to the predicted values (The processing constant M is in this case taken 2). Table II summarizes some typical results for the traditional FDA, the FSD ($t_{ox} = 1$ μm), and the DSFSD ($t_{ox} = 0.1$ μm).

VI. CONCLUSION

A new DSFSD is presented. It has an excellent signal-to-noise ratio, because it has a low thermal noise and produces no kTC noise. A low-capacitance resistor, integrated in the p well of the CCD is used as load. The theory and modeling of the DSFSD have been described using a new model.

APPENDIX A

$$I = \frac{E(x)Wd_c}{\rho(x)} = -q\mu_p p\frac{\partial V(x)}{\partial x}Wd_c = -\mu_p\sigma(x)W\frac{\partial V(x)}{\partial x}. \tag{A.1}$$

The charge per area as a function of x is given by

$$\sigma(x) = C_{\mathrm{pc}_\square}(V(x) - V_p) + C_{\mathrm{gc}_\square}(V(x) - V_g). \tag{A.2}$$

Integration over the total transistor length results in

$$I = \frac{1}{L}\int_0^L Idx$$

$$= -\mu_p\frac{W}{L}\int_0^L [C_{\mathrm{pc}_\square}(V(x) - V_p) + C_{\mathrm{gc}_\square}(V(x) - V_g)] \times \frac{\partial V(x)}{\partial x}dx \tag{A.3}$$

$$= -\mu_p\frac{W}{L}\int_0^{V_{\mathrm{ds}}} dV[C_{\mathrm{pc}_\square}(V - V_{\mathrm{ps}}) + C_{\mathrm{gc}_\square}(V - V_{\mathrm{gs}})] \tag{A.4}$$

$$= -\mu_p\frac{W}{L}\left[(C_{\mathrm{pc}_\square}+C_{\mathrm{gc}_\square})\frac{V^2}{2} - (C_{\mathrm{pc}_\square}V_{\mathrm{ps}}+C_{\mathrm{gc}_\square}V_{\mathrm{gs}})V\right]_0^{V_{\mathrm{ds}}} \tag{A.5}$$

$$= -\mu_p\frac{W}{L} \times \left((C_{\mathrm{pc}_\square} + C_{\mathrm{gc}_\square})\frac{V_{\mathrm{ds}}^2}{2} - (C_{\mathrm{pc}_\square}V_{\mathrm{ps}} + C_{\mathrm{gc}_\square}V_{\mathrm{gs}})V_{\mathrm{ds}}\right) \tag{A.6}$$

$$\mu_p\frac{W}{L}\left((C_{\mathrm{pc}_\square}V_{\mathrm{ps}} + C_{\mathrm{gc}_\square}V_{\mathrm{gs}})V_{\mathrm{ds}} - (C_{\mathrm{pc}_\square} + C_{\mathrm{gc}_\square})\frac{V_{\mathrm{ds}}^2}{2}\right) = \mu_p\frac{W}{L}\left(\eta V_{\mathrm{ds}} - \xi\frac{V_{\mathrm{ds}}^2}{2}\right)$$

where

$$\eta \equiv C_{\mathrm{pc}_\square} V_{\mathrm{ps}} + C_{\mathrm{gc}_\square} V_{\mathrm{gs}} \quad \text{and} \quad \xi \equiv C_{\mathrm{pc}_\square} + C_{\mathrm{gc}_\square}. \tag{A.7}$$

APPENDIX B

$$\begin{aligned} Q_{\mathrm{cp}} &= -\frac{C_{\mathrm{pc}_\square}}{L}\int_0^L (V_p - V(x))dx \\ &= -\frac{C_{\mathrm{pc}_\square}}{L}\int_0^{V_{\mathrm{ds}}} \frac{dV}{\frac{dV}{dx}}(V_{\mathrm{ps}} - V(x)) \\ &= -\frac{C_{\mathrm{pc}_\square}}{L}\int_0^{V_{\mathrm{ds}}} \frac{(V_{\mathrm{ps}} - V(x))}{I}\mu_p W\sigma(x)dV \end{aligned} \tag{B.1}$$

$$\begin{aligned} &-\frac{\mu_p}{I}\frac{W}{L}C_{\mathrm{pc}_\square}\int_0^{V_{\mathrm{ds}}} [V_{\mathrm{ps}} - V(x)] \\ &\quad \times [C_{\mathrm{pc}_\square}(V(x) - V_{\mathrm{ps}}) + C_{\mathrm{gc}_\square}(V(x) - V_{\mathrm{gs}})]dV \end{aligned} \tag{B.2}$$

$$\begin{aligned} &-\frac{\mu_p}{I}\frac{W}{L}C_{\mathrm{pc}_\square}\int_0^{V_{\mathrm{ds}}} -(C_{\mathrm{pc}_\square} + C_{\mathrm{gc}_\square})V^2(x) \\ &\quad + [V_{\mathrm{ps}}(C_{\mathrm{pc}_\square} + C_{\mathrm{gc}_\square}) \\ &\quad\quad + (C_{\mathrm{pc}_\square}V_{\mathrm{ps}} + C_{\mathrm{gc}_\square}V_{\mathrm{gs}})]V(x) \\ &\quad - V_{\mathrm{ps}}(V_{\mathrm{ps}}C_{\mathrm{pc}_\square} + V_{\mathrm{gs}}G_{\mathrm{gc}_\square})dV \end{aligned} \tag{B.3}$$

$$= -\frac{2\xi}{\eta^2}C_{\mathrm{pc}_\square}\left(-\frac{\xi V_{\mathrm{ds}}^3}{3} + (V_{\mathrm{ps}}\xi + \eta)\frac{V_{\mathrm{ds}}^2}{2} - V_{\mathrm{ps}}\eta V_{\mathrm{ds}}\right) \tag{B.4}$$

where

$$V_{\mathrm{ds}}^{\mathrm{sat}} = \frac{\eta}{\xi}$$

this results in

$$Q_{cp} = -\frac{2}{\eta}C_{\mathrm{pc}_\square}\left(-\frac{\eta^2}{3\xi} + \frac{V_{\mathrm{ps}}\eta}{2} + \frac{\eta^2}{2\xi} - \eta V_{\mathrm{ps}}\right) \tag{B.5}$$

$$= -\frac{2}{\eta}C_{\mathrm{pc}_\square}\left(\frac{\eta^2}{6\xi} - \frac{\eta V_{\mathrm{ps}}}{2}\right) \tag{B.6}$$

$$= C_{\mathrm{pc}_\square}\left(V_{\mathrm{ps}} - \frac{V_{\mathrm{ds}}}{3}\right) \tag{B.7}$$

by analogy

$$Q_{\mathrm{cg}} = -\frac{C_{\mathrm{gc}_\square}}{L}\int_0^L (V_g - V(x))dx = C_{\mathrm{gc}_\square}\left(V_{\mathrm{gs}} - \frac{V_{\mathrm{ds}}}{3}\right). \tag{B.8}$$

Summation of (B.7) and (B.8) results in

$$Q_c = -\frac{2}{3}\eta \tag{B.9}$$

APPENDIX C

According to the small-signal diagram (Fig. 5) at node V_p

$$j\omega Q = j\omega C_1 V_p + j\omega C_2(V_p - V_s) \tag{C.1}$$

$$\Rightarrow Q = V_p(C_1 + C_2) - V_s C_2 \tag{C.2}$$

where

$$C_1 \equiv C_{pN} + C_{\mathrm{pd}}^0 = \frac{C_{\mathrm{ps}}C_{\mathrm{gs}}}{2(C_{\mathrm{ps}} + C_{\mathrm{gs}})} \quad \text{and} \quad C_2 \equiv C_{\mathrm{ps}} + C_{\mathrm{ps}}^0.$$

According to the small-signal diagram, the gain $A(\Delta V_s/\Delta V_p)$ is

$$A = \frac{g_p + j\omega C_2}{g_p + g_m + j\omega(C_2 + C_3)} \tag{C.3}$$

with

$$C_3 \equiv C_{\mathrm{gs}} + C_{\mathrm{gs}}^0.$$

The cross-over frequency is approximately 2 GHz. This means that for this application only the low-frequency part is important. Therefore A_0 can be used, instead of A.

$$A_0 = \frac{g_p}{g_p + g_m} = \frac{C_{\mathrm{pc}}}{C_{\mathrm{pc}} + C_{\mathrm{gc}}} \tag{C.4}$$

$$Q = \frac{V_s}{A_0}(C_1 + C_2) - V_s\frac{A_0}{A_0}C_2 \tag{C.5}$$

substitution of $Q = -qN_{el}$ gives for the responsivity

$$\mathrm{resp} \equiv \frac{\Delta V_s}{\Delta N_{el}} = -\frac{qA_0}{C_1 + C_2(1 - A_0)} = -\frac{qA_0}{C_{in}} \tag{C.6}$$

with

$$C_{in} = C_1 + C_2(1 - A_0).$$

APPENDIX D

According to Fig. 5

$$i_n + g_m V_{\mathrm{gs}} + g_p V_{\mathrm{ps}} + j\omega C_2(V_s - V_p) + j\omega C_3 V_s = 0. \tag{D.1}$$

Because only the low-frequency terms are important, the capacitive currents are approximately 0. This results in

$$i_n \approx (g_p + g_m)V_s - g_p V_p \tag{D.2}$$

$$\frac{i_n}{g_p} = \frac{V_s}{A_0} - V_p. \tag{D.3}$$

With respect to the noise source, the node V_p is floating. The potential V_p is therefore completely determined by the source potential and capacitance weighting factors.

$$V_p = \frac{C_2}{C_1 + C_2}V_s = \frac{C_2}{C_t}V_s. \tag{D.4}$$

Combination of (D.3) and (D.4) results in

$$\frac{i_n}{g_p} = \frac{C_t V_s}{A_0 C_t} - \frac{A_0 C_2}{A_0 C_t}V_s = -\frac{V_s q}{\mathrm{resp}C_t} \tag{D.5}$$

from which the source noise-voltage squared is

$$\langle V_{s_n}^2 \rangle = \frac{\langle i_n^2 \rangle \mathrm{resp}^2 C_t^2}{q^2 g_p^2} = \frac{\langle i_n^2 \rangle}{g_p^2}A_0^2\left(\frac{C_t}{C_{in}}\right)^2. \tag{D.6}$$

REFERENCES

[1] J. T. Bosiers, H. L. Peek, A. C. Kleimann, N. J. Daemen, E. Roks, A. G. van der Sijde, R. M. Jansen, and P. Opmeer, "A S-VHS compatible 1/3″ 720(H)* 588(V) FT CCD with low dark current by surface pinning," *IEDM Tech. Dig.*, pp. 97–100, 1992.

[2] P. Centen, "CCD on-chip amplifiers: Noise performance versus MOS transistor dimensions," *IEEE Trans. Electron Devices*, vol. 38, no. 5, pp. 1206–1216, May 1991.

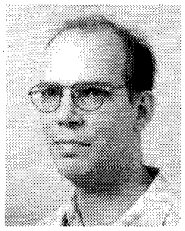
[3] R. J. Brewer, "The low light level potential of a CCD imaging array," *IEEE Trans. Electron Devices*, vol. ED-27, no. 2, Feb. 1980.

[4] Y. Matsunaga, S. Oosawa, M. Iesaka, S. Manabe, N. Harada, and N. Suzuki, "A high sensitivity output amplifier for CCD image sensor," *IEDM Tech. Dig.*, pp. 116–119, 1987.

[5] E. Roks, P. G. Centen, L. Sankaranarayanan, J. T. Bosiers, and W. F. Huinink, "A bipolar floating-base detector (FBD) for CCD image sensors," *IEDM Tech. Dig.*, pp. 109–112, 1992.

[6] J. G. C. Bakker, "Simple analytical expressions for the fringing field and fringing field induced transfer time in charge-coupled devices," *IEEE Trans. Electron Devices*, vol. ED-38, no. 5, pp. 1152–1161, May 1991.

[7] H. C. de Graaff and F. M. Klaassen, *Compact Transistor Modeling for Circuit Design* Wien: Springer-Verlag, 1989, pp. 243–244.



Edwin Roks (M'90) was born in Breda, The Netherlands, on July 5, 1964. He received the B.Sc. degree in electrical engineering from the College of Advanced Technology, Breda, in 1985, the M.Sc. degree in electrical engineering from the University of Technology, Eindhoven in 1990, and the Ph.D. degree from Twente University, The Netherlands, in 1990.

In 1985, he entered military service, where he became an officer and lectured on telecommunications at the Royal Military Academy, The Netherlands. In 1989, he joined Philips Research Laboratories, Eindhoven, first as a student in the semiconductor laser group, where he worked on single-mode semiconductor lasers for coherent fiber-communication, and later as a member of the scientific staff of the CCD research group, Philips Imaging Technology. Since 1993, he has been project leader of several high resolution imaging projects Apart from this work, his current research interests concerns CCD image sensors, especially low noise output circuitry and methods form dark current reduction.

Peter G. M. Centen was born in Goirle, The Netherlands, on October 19, 1952. He received the Master's degree in electronics (cum laude) from the Eindhoven Institute of Technology, Eindhoven, The Netherlands.

In 1983, he became an assistant researcher and worked on a variational principle for the equilibrium conditions for a magneto-hydro-dynamic plasma. He joined Philips Broadcast Television Systems, Breda, The Netherlands, in late 1984, carrying out research on optimal signal processing for CCD sensors. As guest researchers at Philips Labs, Eindhoven, he devoted his attention to noise reduction and high speed operation of the CCD sensor output circuitry. He was involved in the development of HDTV and switchable 4:3/16:9 SDTV cameras. He is presently involved in both SDTV and customer defined CCD-sensor application (OEM) for optimal CCD-sensor usage.

Jan T. Bosiers (M'81) was born in Mortsel, Belgium, in 1956. He graduated as Electronic Engineer from the Katholieke University of Leuven, Belgium, in 1980.

From 1980 to 1984, he was a research scientist at he ESAT Laboratory, Department of Electronic Engineering, Katholieke University of Leuven, working on the development of high-resolution linear CCD imagers. From 1985 to 1986, he was a consulting engineer, U.S. Naval Research Laboratory, Washington, D.C., working on the research and development of deep-depletion, backside-illuminated CCD's for detection of UV-en X-rays. Since October 1986, he has been with Philips Research Laboratory, Eindhoven, the Netherlands. In the research group of Philips Imaging Technology, he has led research and development of several new CCD imagers for consumer and medical applications. He is presently in charge of the research of novel CCD imager structures.

Wim F. Huinink was born in Gemert, The Netherlands, on May 13, 1960. He received the teaching degree in physics and mathematics from the N.L.O. at Nijmegen, The Netherlands, in 1986.

He then joined Philips Research Laboratories, Eindhoven, The Netherlands, where he has worked on device and process characterization of several MOS processes. In 1991, he became a member of the CCD research group, Philips Imaging Technology. His current work is design and testing of CCD image sensors for broadcast cameras.