A BIPOLAR FLOATING BASE DETECTOR (FBD) FOR CCD IMAGE SENSORS

Edwin Roks, Peter G. Centen, L. Sankaranarayanan,
Jan W. Slotboom, Jan T. Bosiers, Wim F. Huinink

Philips Research Laboratories Eindhoven - WAG-1
P.O. Box 80 000, 5600 JA Eindhoven, The Netherlands
Phone +31-40-742170 - Fax +31-40-743390

ABSTRACT

A new bipolar charge detector, called the Floating Base Detector (FBD), fabricated in a standard CCD image sensor process, is presented. It can be used as an output structure for CCD registers or as a compact pixel-gain element. The FBD, with a charge handling capability of 30,000 electrons, has achieved a dynamic range of 84 dB over 5 MHz bandwidth which corresponds to a noise electron equivalent of 1.9 electrons.

INTRODUCTION

The noise of today's imagers is dominated by dark current and amplifier noise. Since we are able to reduce the dark current significantly e.g. by means of surface pinning techniques [1], the demand for low noise amplifiers increases. The traditional Floating Diffusion Amplifier (FDA) has a relative high noise level, because its sensing capacitance cannot be sufficiently small. To reduce this capacitance, a number of detectors are known in which the amplifier is partly integrated with the CCD channel. One of these structures is called the Floating Surface Detector (FSD). The FSD uses the principle of straddling a p-channel MOS transistor in surface mode over an n-type buried channel CCD output-register to achieve a high sensitivity and was first presented by Brewer [2]. Matsunaga et al. [3] later adapted the FSD for CCD structures with a vertical overflow drain. Yamashita et al. [4] also used the FSD as a pixel-gain element in a common-source configuration for a large area photo-array. In our paper the feasibility to integrate a bipolar transistor with an FSD in common-source configuration to achieve an extra current gain is demonstrated. This new detector will be referred to as the Floating Base Detector (FBD). The drain of the sensing p-MOS transistor forms the floating base of a bipolar npn-transistor. The bipolar transistor is integrated vertically so that an amplification of the sensed signal charge is achieved without sacrificing chip area. This is important when the FBD is used as a pixel-gain element. A high current gain together with the low output impedance of the integrated amplifier increases the driving capability compared to the FSD.

DEVICE STRUCTURE AND OPERATION

A. Structure

To characterize the FBD a test-structure was designed, as illustrated in Fig. 1.

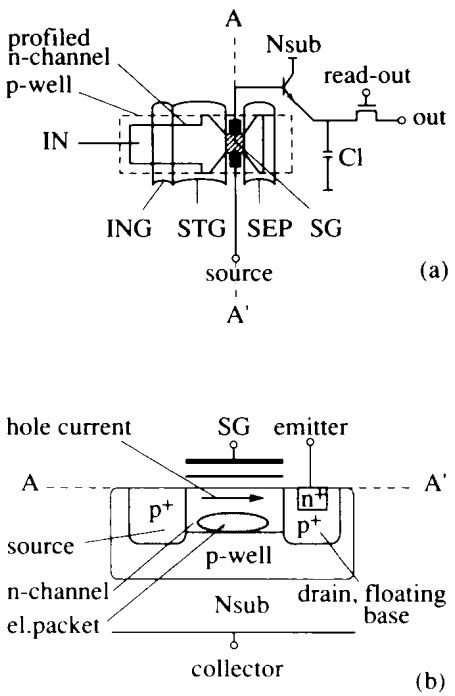

Fig 1: (a) Topview of test-structure of the Floating Base Detector (FBD). (b) Cross-section of the FBD, showing the vertically integrated npn-transistor.

0-7803-0817-4/92 $3.00 © 1992 IEEE

It consists of an electrical input diffusion (IN), an input gate (ING), a storage gate (STG), an FBD, and a blocking separation gate (SEP). The device is made in a standard CCD process with an additional self-aligned, high-energy phosphorus implant under the sensing gate (SG) to create a dual channel in the silicon. The potential profile required for a surface channel for holes and a bulk channel for collection of the signal electrons is shown in Fig. 2.

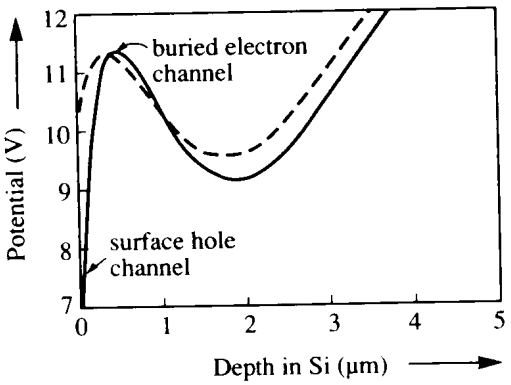

Fig 2: Potential profile under sensing gate (solid curve) and storage gate (dashed curve).

Fig. 3 shows the layout of the FSD, together with the results of a 3-dimensional device simulation. The butterfly structure of the FSD ensures excellent confinement of electrons and holes under the STG and SG. The width (W) and length (L) of the p-MOS transistor of the FBD are 4 μm and 6 μm respectively. The emitter-area is 24 μm^2. The layout of the FBD is shown in Fig. 4.

B. Operation

The signal electrons, injected by the input diffusion, are integrated under the storage gate (see Fig. 1). These electrons can be transferred under the sensing gate by clocking the storage gate negative. The presence of these signal electrons in the bulk modulates the surface potential which in turn determines the threshold voltage of the p-MOS transistor, and hence the turn-on current of the MOS transistor. By pulsing the source of the p-MOS transistor, holes are pumped through the surface channel into the base of the bipolar and back, thereby turning the bipolar momentarily on. A 2-dimensional dynamic simulation (CURRY) shows that the hole current is linear with the amount of signal electrons. The output emitter current pulse, which is the β times amplified base current, is used to drive the load capacitance. This amplified charge is now read out through a p-channel read-out transistor. Both p-MOS transistor and bipolar transistor are switched off and automatically reset for the next charge packet. Contrary to

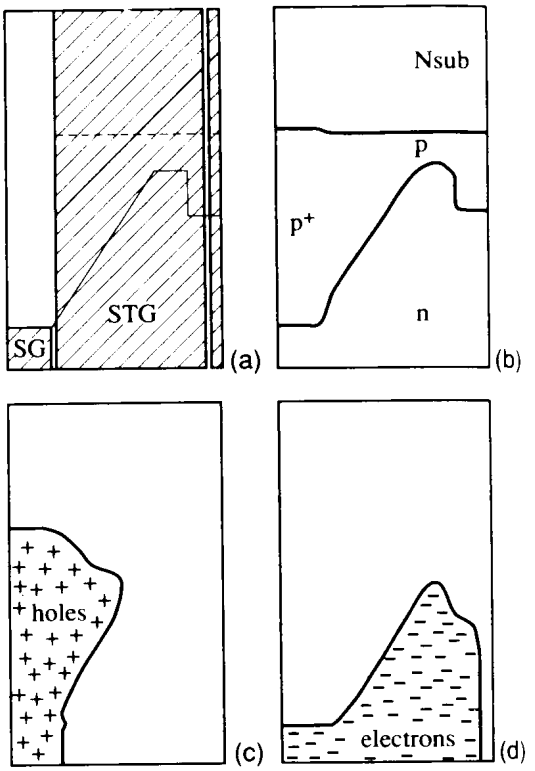

Fig 3: 3-Dimensional device simulation (PADDY) of the Butt structure of the Floating Surface Detector. (a) Gate structure Dopant structure at surface. (c) Hole concentration at surface Electron concentration in bulk channel.

floating node schemes precharging is not necessary. A detection, the signal electrons are drained into the subst by applying a negative pulse on all gates. The thermal n of the FSD is very low, so that the total noise of the F is only determined by the shot noise of the base current kTC-noise of the p^+ drain of the FSD.

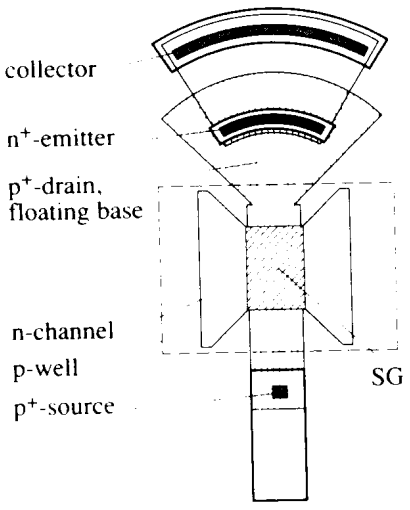

Fig 4: Layout of Floating Base Detector (FBD).

EVALUATION AND RESULTS

The clock scheme used for characterization of the FBD is shown in Fig. 5. The improvement in terms of driving capacity and feed-through immunity obtained using the integrated bipolar transistor (FBD) is shown in figure 6 with reference to the same structure but without the bipolar (FSD). Both structures use the same load resistance (R). The current gain (β) of the bipolar was measured to be 265. The maximum charge handling capability measured was 20,000 to 30,000 electrons for various dopant profiles. For noise and responsivity measurements a load resistance of 4.7 kΩ was used. The linear output characteristic is illustrated in Fig. 7. The output voltage and the noise voltage $<e_n>$ were measured as a function of the base current I_b, since this current is linearly dependent on the number of injected signal electrons under the sensing gate. The results of these measurements are shown in Fig. 8 where both the output voltage, proportional to the base current I_b, and the noise voltage $<e_n>$, proportional to $\sqrt{I_b}$, are given. This proportionality confirms our expectation that shot noise of the base current is the dominant noise source. It can be described by the relation

$$<e_n> = \sqrt{2qI_b}\ \beta R \qquad (1)$$

The result of this formula is also plotted in Fig. 8. It fits with the noise measurements. The dynamic range is defined as the maximum output voltage, divided by the cross-over noise level of thermal noise and shot noise. This noise level is given by the thermal noise of the overall circuitry when the FBD is in off-state. It is measured as 14 nV/√Hz. The dynamic range is given by

$$Dyn.Range = 20.\log\left(\frac{V_{sat}}{<e_n>_{th}\sqrt{B.<M>}}\right) \qquad (2)$$

In this expression V_{sat}, $<e_n>_{th}$, B, and $<M>$ are respectively, the maximum output voltage, the thermal noise floor, the bandwidth, and a multiplication factor that gives the average increase of noise due to processing when a white noise source is input to the signal processing. For a single output $<M>$ equals 4 [5]. With our values of $<e_n>_{th}$ and V_{sat} this results in a dynamic range of 84 dB within a bandwidth of 5 MHz.

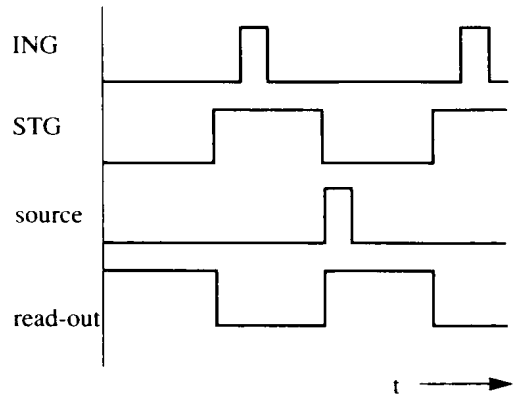

Fig.5: Clocking scheme for characterization of the Floating Base Detector.

CONCLUSION

This paper describes a new device which consists of the combination of a bipolar transistor and a Floating Surface Detector for application to CCD imagers as an output amplifier. It offers a high output sensitivity, a charge handling capability of 30,000 electrons, and an equivalent noise level of less than 2 electrons within a bandwidth of 5 MHz. This corresponds to a dynamic range of 84 dB.

ACKNOWLEDGEMENT

The authors would like to thank their colleagues from the Microcircuits group and FABWAG especially P. Kranen and E.J.M. Daemen for processing of the devices and A. Heringa from the Applied Mathematics Group for assistance with the device simulations.

REFERENCES

[1] Bosiers, J.T., et al.
A S-VHS compatible 1/3" 720(H) * 588(V) FT-CCD with low dark current by surface pinning.
IEDM Tech. Dig., 1992.

[2] Brewer, R.J.
A low noise CCD output amplifier.
IEDM Tech. Dig., 1978, p. 610.

[3] Matsunaga Y., et al.
A high sensitivity output amplifier for CCD image sensor.
IEDM Tech. Dig., 1987, p. 116.

[4] Yamashita, H., Y. Matsunaga, M. Iesaka, S. Manabe, and N. Harada
A new high sensitivity photo-transistor for area image sensors.

IEDM Tech. Dig., 1988, p. 78.

[5] Centen, P.
CCD on-chip amplifiers: Noise performance versus MOS transistor dimensions.
IEEE Trans. Electron Devices, vol. 38, no. 5, May 1991, p. 1206.

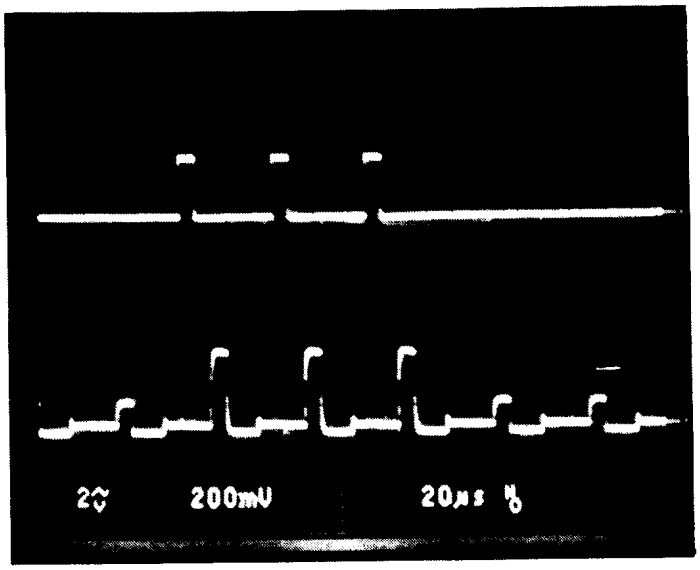

Fig 6a: Output FSD (200 mV/div) for a set of three input pulses.

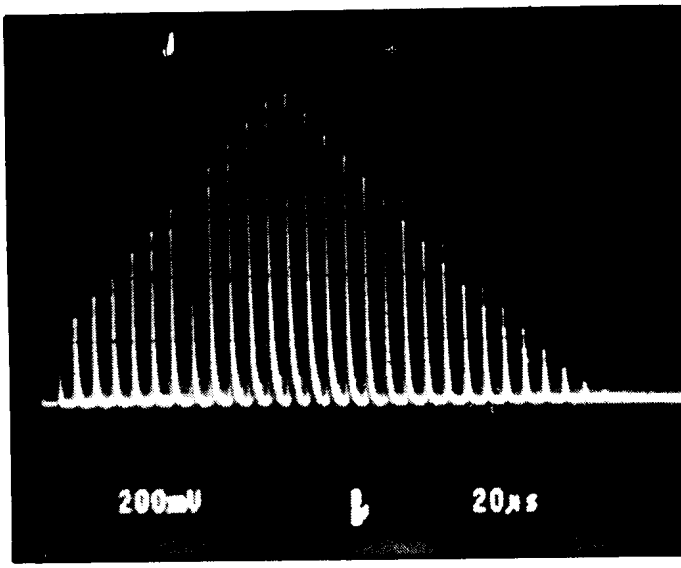

Fig 7: FBD output for set of source pulses with triangular envelop

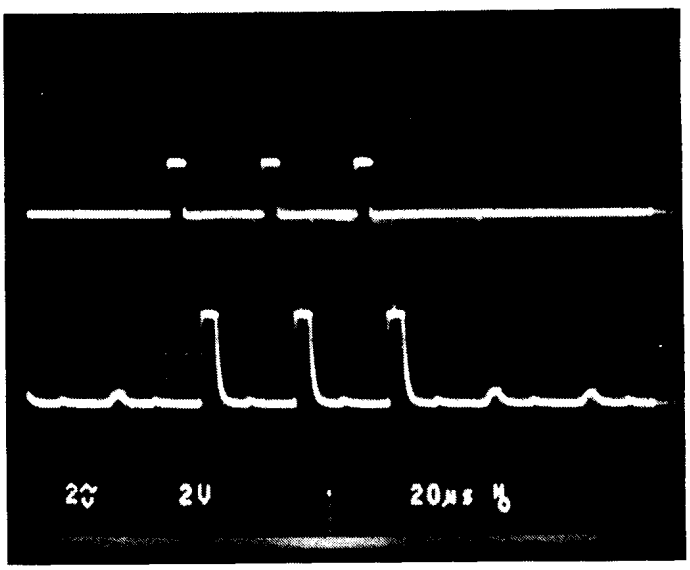

Fig 6b: Output FBD (2V/div) for a set of three input pulses.

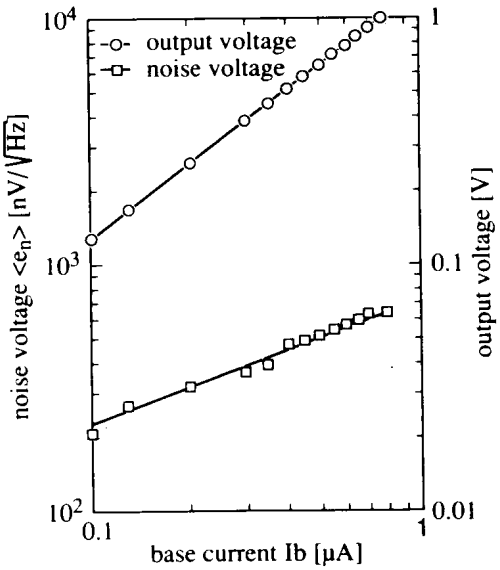

Fig 8: Output voltage and noise voltage as a function of the FBD ba current