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A RESET NOISE-FREE HIGH-SPEED READ-OUT MODE FOR A FLOATING-DIFFUSION DETECTOR WITH RESISTIVE FEEDBACK

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Abstract

A different mode of operating the floating-diffusion detection node is investigated. This new mode has no reset noise and therefore no need for reset noise suppression. The demand on the bandwidth of the on-chip amplifier is relaxed from about 3 times the pixel rate, a minimum requirement to suppress reset noise sufficiently, to about half the pixel rate. The time needed to dump the charge on the floating diffusion can also be relaxed from the order of nanoseconds to half the pixel clock time. The optimal signal processing is an ordinary low-pass filter.

It will be shown that in the resistive feedback mode one can maintain equal or better noise performance than with time-discrete signal processors such as integrate and dump or correlated double sampling or any other signal processing.

Keywords: noise, optimal signal processing, CCD, imagers, high-speed read-out, HDTV, correlated double sampling, integrate and dump, clamp sample, floating diffusion, resistive feedback, noise electron density.

1. Introduction

The flow of charge through the horizontal register of a solid-state image sensor can be regarded either as a series of charge packets or as a current. In the first case one uses a capacitor to convert charge into a voltage and in the second case a resistor. In many CCD imagers the choice is made to use a floating diffusion for the capacitor which must be reset after each charge packet.

In high-speed devices where charge is clocked at high speed it is also very difficult to design a good signal processor. To give an example, suppose that the horizontal register is clocked at 72 MHz. One clock interval has a period time of 13.9 ns, with 6.9 ns for the video signal (50% duty cycle), 4.6 ns for the reset noise hold level, and 2.3 ns for switching the reset FET on. Generating the necessary pulses which have rise and fall times of less than a nanosecond and which have proper timing is a problem. When using a resistor to convert a current into a voltage no special timing is required and signal processing consists only of a low-pass filter.

The intent of this feasibility study is to investigate whether using the current output is a good alternative to a floating-diffusion scheme in high-speed applications.

The present state of the art in on-chip amplifier design is such that the contribution of the $1/f$-noise to the signal-to-noise ratio is negligible. In imager applications one still needs an easy-to-build slow-clamp to remove the low-frequency disturbances caused by the $1/f$-noise. This filtering is automatically included in the correlated double sampling or integrate and dump signal processors.

2. Destructive charge readout using a floating-diffusion and reset FET

The traditional floating-diffusion configuration[1,2]) for reading out charge packets is extensively described in any textbook on CCD sensors and can also be found in this issue[3]). Figure 1 shows the basic elements of the output stage, including the capacitance between the input of the on-chip amplifier and ground. C, at the floating diffusion, is the charge sensing capacitance. The voltage source e_n represents the equivalent noise of the on-chip amplifier at the input. The current source i represents the charge dumped (qN) on the floating diffusion; for one charge packet the following relation holds

$$\int_{-\infty}^{\infty} i(t)\mathrm{d}t = qN \tag{1}$$

with q the unit charge of one electron and N the number of electrons in one charge packet.

The charge packet is transported through the CCD-register with a clock frequency f_h. Therefore every clock period $T_h = 1/f_h$ charge is dumped at the detection node.

When the detection node capacitor (C) has received a charge packet the reset FET will clamp (reset) the capacitance to a reference potential V_{ref}. This prepares the capacitor (C) to receive the next charge packet. During this clamping reset noise is generated[2]).

This reset noise can reach high values, as much as an equivalent of 40 electrons. Signal processing, such as correlated double sampling, integrate and dump, delay line processing, clamp sample[4]) and so forth, is needed to

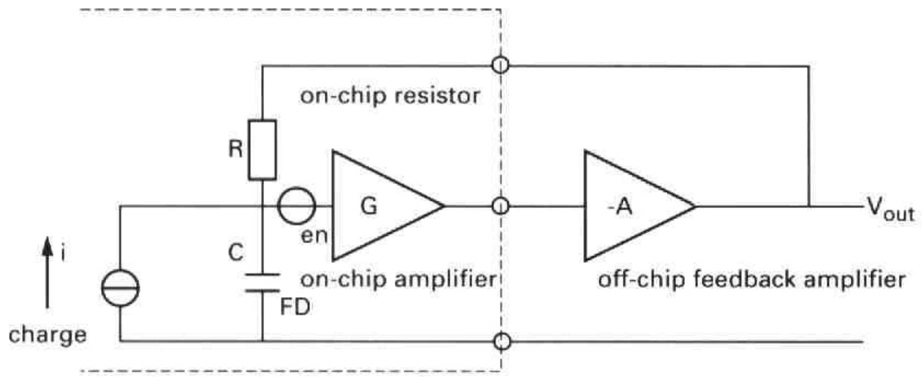

Fig. 1. The resistive feedback read-out mode. On-chip are the amplifier with gain G, the resistor R and the floating diffusion with capacitance C. Off-chip is the negative feedback amplifier with gain $-A$ together with part of the feedback loop. The reset FET is replaced by the resistor R as compared with the traditional concept of a floating-diffusion detector.

suppress the reset noise and to obtain reasonable noise levels. In many cases the signal is resampled at a hold capacitance resulting in a $\sin x/x$ spectrum.

The noise voltage at the output of the on-chip amplifier (Ge_n) divided by the output voltage due to one electron (Gq/C is called the responsivity) squared gives an easier quantity to calculate noise performance. Its dimension is $e^2\ \mathrm{Hz}^{-1}$ and it is called the noise electron density (NED)[5].

It is shown[4]) that the noise limit which can be obtained with optimal[1] filtering is

$$S_{\mathrm{proc}}(f) = M\left(e_n \frac{C}{q}\right)^2 \mathrm{sinc}^2\left(\frac{f}{f_h}\right) \tag{2}$$

Without going into details, the signal processor's figure of merit (M) for the optimal filter, a dimensionless quantity, for a single-output CCD is

$$M = \frac{T_h}{T_v} + \frac{T_h}{T_{rs}} = 5 \tag{3}$$

In this equation the different times are respectively: T_h the inverse of the horizontal clock frequency, $T_h = 1/f_h$; T_v the time video is available (the time charge is held at capacitor C), usually $T_h/2$; T_{rs} the reset hold level, usually about $T_h/3$.

The integrate and dump processing is the optimal processing[4,6]). The integrate action gives the optimal filtering and the dump a $\sin x/x$ spectrum.

[1]Optimal is defined as minimizing the noise after filtering with the constraints that the reset noise is fully suppressed and the resolution stays the same. The solution is the two-slope integrator: one slope integrates the reset noise and the second slope the signal + reset noise. It is also called integrate and dump.

In practice it is very difficult to build an optimal signal processor for high speed and the figure of $M = 5$ will not be met. A value between 5 and 10 is more realistic.

The number of equivalent noise electrons after signal processing N_{proc} within a bandwidth B is

$$\int_0^B M\,\text{NED}\,\text{sinc}^2\left(\frac{f}{f_\text{h}}\right)\text{d}f \tag{4}$$

with

$$\text{NED} = \left(\frac{e_\text{n}C}{q}\right)^2 \tag{5}$$

The NED is the noise spectral density expressed in such a way that it leads to a natural description of the noise in CCDs. The number of noise electrons in which the noise is expressed frequently only has a meaning *after* signal processing and only in a given bandwidth, while the noise electron density has a meaning already at the CCD-output without signal processing.

In general, the detection-node capacitance is distributed between passive and active elements, and the capacitance C must be replaced by the total capacitance of the detection node[5]).

To make a fair comparison between the two methods their resolution must be made the same. The choice is made to compensate the frequency response in such a way that a flat frequency response up to half the sample frequency is obtained. The response to a Dirac impulse is $\sin x/x$. However, since the noise spectrum also has a $\sin x/x$ shape the compensation will flatten the noise spectrum. Its noise power expressed in equivalent noise electrons equals

$$N_{\text{proc}}^2 = M\left(\frac{e_\text{n}C}{q}\right)^2 B \tag{6}$$

3. Destructive charge read-out using a resistive feedback

The resistive feedback mode needs an on-chip high ohmic resistor in the same position as the well-known reset transistor (fig. 1) and an (off-chip) invertor stage ($-A$) for the feedback.

The use of a resistor to convert charge into voltage is a very old one, just as the well-known floating-diffusion detector with on-chip amplifier[1,2,3,7]) is.

What is new is the feedback of the output voltage of the on-chip amplifier by an on-chip resistor. The resistor is placed on-chip because an off-chip resistor increases the capacitance C from tens of femtofarads to the order of picofarads charge packet of 1 electron per pixel (the responsivity):

$$\text{Resp} = H(0)\frac{q}{T_{\text{h}}} = H(0)qf_{\text{h}} = -\frac{AG}{1+AG}Rqf_{\text{h}} \tag{13}$$

The noise electron density for the feedback mode is

$$\text{NED}(f)_I = \frac{1}{q^2 f_{\text{h}}^2}\left(\frac{4kT}{R} + \frac{e_{\text{n}}^2}{R^2}[1 + (2\pi fRC)^2]\right) \tag{14}$$

The equivalent number of noise electrons for the noise power in a bandwidth B is

$$N_I^2 = \int_0^B \text{NED}(f)_I \mathrm{d}f = \frac{4kT}{q^2 f_{\text{h}}^2 R}B + \left(\frac{e_{\text{n}}}{qf_{\text{h}}R}\right)^2 B + \left(\frac{e_{\text{n}}C}{q}\right)^2 \left(2\pi\frac{B}{f_{\text{h}}}\right)^2 \frac{B}{3} \tag{15}$$

4. Discussion

The integrate and dump has a noise spectrum which after compensation is flat, whereas the resistive feedback mode has a triangular noise spectrum (14) after frequency compensation, see fig 2.

In the case of an image sensor one has the benefit of the fact that at equal noise power the subjective evaluation of the noise in the resistive feedback mode is even better owing to the triangular shape of the noise spectrum and the fact that the human eye is less sensitive for noise at high spatial frequencies.

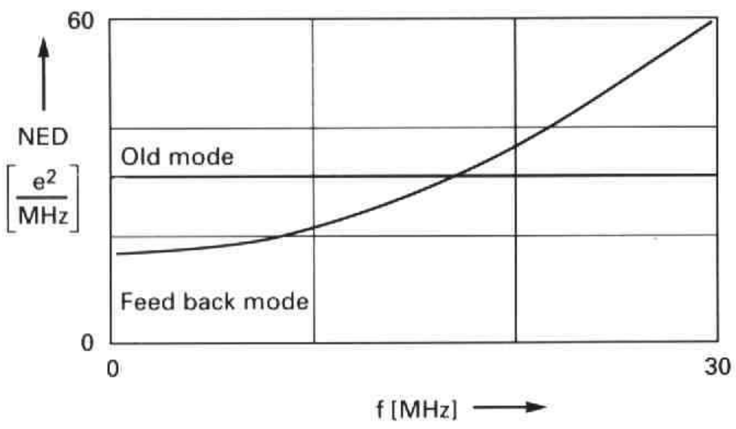

Fig. 2. Noise spectrum after integrate and dump with $M = 5$ and flat frequency compensation, and after the resistive feedback mode with a triangular-shaped spectrum. The noise power in a bandwidth up to half the pixel rate is the same in both cases. Notice the much lower noise level at lower frequencies for the resistive feedback read-out mode compared with integrate and dump.

The ratio between the noise electrons in both cases—the noise electrons in the resistive feedback case (15) divided by the noise electrons in the traditional case (6)—is

$$\frac{N_I^2}{N_{\mathrm{proc}}^2} = \frac{4kTR}{f_{\mathrm{h}}^2 R^2 C^2 M e_{\mathrm{n}}^2} + \frac{1}{f_{\mathrm{h}}^2 R^2 C^2 M} + \frac{4\pi^2}{3M}\left(\frac{B}{f_{\mathrm{h}}}\right)^2 \tag{16}$$

Clearly the rightmost term is only determined by the ratio between the bandwidth and the clocking frequency (B/f_{h}). This ratio will always be smaller then 1/2 since no signal reconstruction is possible for output signals above half the sample rate.

For the resistive feedback mode to be equal or better in signal-to-noise performance it is necessary that the signal processing performance index M is such that

$$M \geqslant \frac{4\pi^2}{3}\left(\frac{B}{f_{\mathrm{h}}}\right)^2 = 3.29 \tag{17}$$

for $B/f_{\mathrm{h}} = 1/2$.

The solution of equation (16) for the resistor value R when the noise ratio between both methods of charge readout equals 1 is

$$R = \frac{4kT}{f_{\mathrm{h}}^2 \mathrm{NED}^2 q^2 M[1 - (4\pi^2/3)(B/f_{\mathrm{h}})^2]} \times \frac{1}{2}\left\{1 + \sqrt{1 + \frac{\mathrm{NED}^4 f_{\mathrm{h}}^2 M}{4(kT/q)^2 (C/q)^2}\left[1 - \frac{4\pi^2}{3}\left(\frac{B}{f_{\mathrm{h}}}\right)^2\right]}\right\} \tag{18}$$

5. Examples

Given a CCD imager, then C, f_{h}, e_{n} and B are fixed and the only degree of freedom left is the choice of the feedback resistor R and the ability to build a good performing signal processor (M).

- Assume an imager with $C = 16$ fF, $f_{\mathrm{h}} = 72$ MHz, $e_{\mathrm{n}} = 25$ nV Hz$^{-1/2}$ and $B = 30$ MHz and an signal processing figure of merit of $M = 5$. Then the value of the feed-back resistor must be at least $R \geqslant 7.1$ MΩ and the responsivity (Rqf_{h}) is 90 μV e^{-1}. With $M = 10$ the feedback resistor must be $R \geqslant 2.5$ MΩ and the responsivity is 32 μV e^{-1}.

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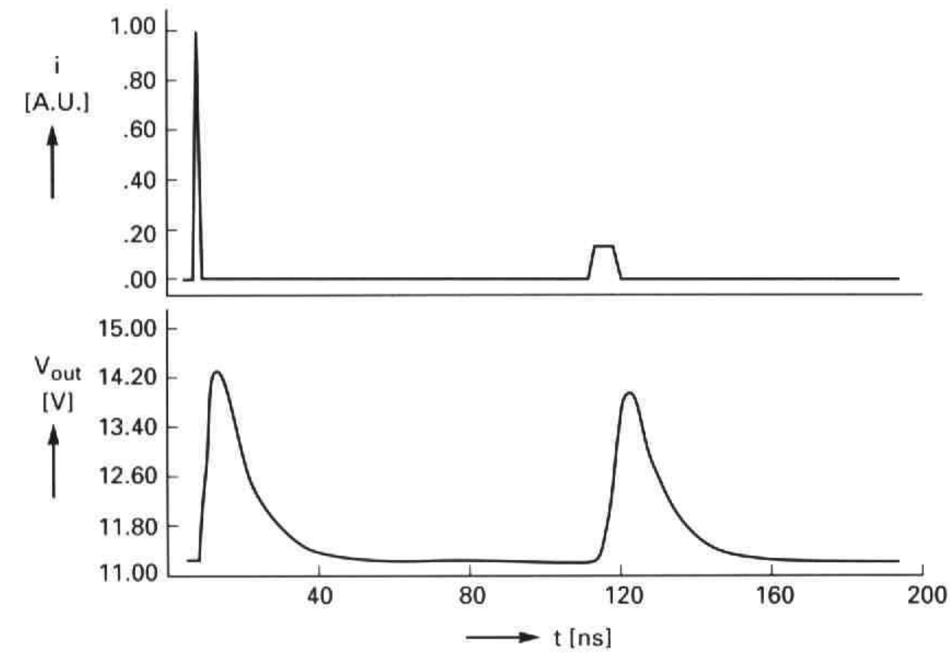


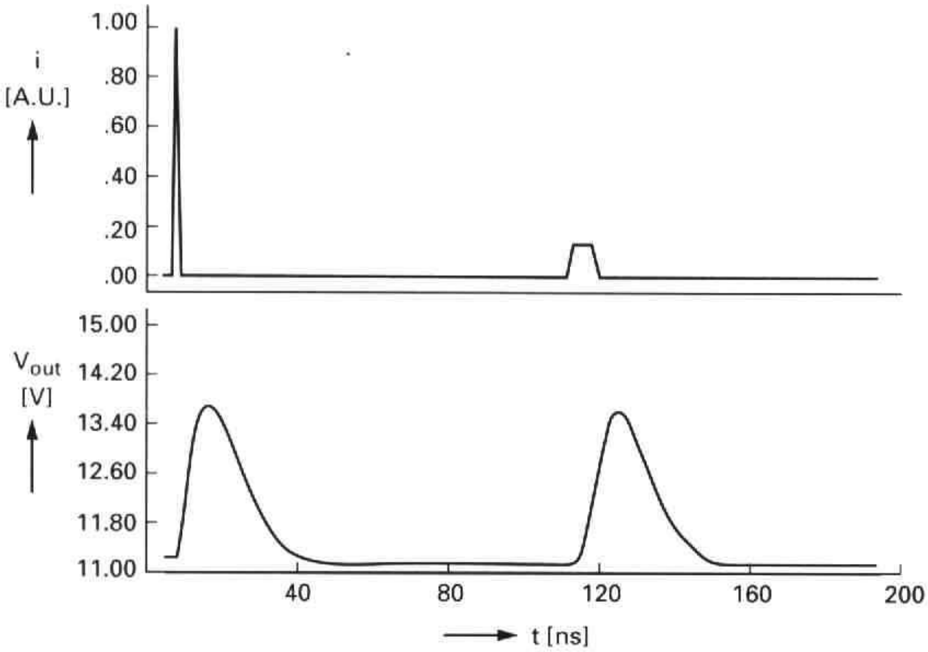
Fig. 3. The output voltage (V_{out}) in the resistive feedback mode as a function of two different current pulses (i) with equal charge content. One has a duration of 1 ns and the other 7 ns. The spacing between the two current pulses is 8 pixels. The bandwidth of the on-chip amplifier is 170 MHz.

- Assume the use of that same imager in progressive mode. Then $f_h = 144$ MHz and $B = 60$ MHz. R must be at least $R \geqslant 1.8$ MΩ to be competitive and the responsivity is 45 μV e^{-1}. With $M = 10$ the resistor value becomes $R \geqslant 0.66$ MΩ with responsivity 17 μV e^{-1}.

For small signals one can even bias the reset transistor in such a way that it emulates the resistor value one needs.

A practical system does not have an infinite gain and the pole-zero combination must be considered. With a correct choice of these time constants and feedback gain A it is possible to shape the output waveform of one pixel to have an almost bandwidth-limited signal to limit the burden on the low-pass filtering.

A simulation of the output voltage with an actual FT-HDTV on-chip amplifier which has a bandwidth of 170 MHz in the one case and a bandwidth of 36 MHz in the other case is shown in fig. 3 and fig. 4. The insensitivity to the duration of the 'charge' pulse and the bandwidth of the on-chip amplifier is clearly seen. In the simulation no compensation is made for the drop in frequency response.



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6. Conclusions

In the resistive feedback mode the old sensing tradition is restored while the benefits of the current designs are retained: a low noise on-chip amplifier with floating-diffusion detector and an on-chip resistor.

It is a concept for reading out charges at high frequencies and maintaining the same or better signal-to-noise ratios as before without the need for complex signal processing schemes. This can come in handy with a progressive-scan HDTV sensor which needs pixel rates of 72 MHz and more.

The benefits of using the resistive-feedback technique lie in the fact that signal processing is continuous and that one needs no time-discrete filtering such as integrate and dump or correlated double sampling with all their difficulties in pulse generation and timing. The rise and fall times no longer play an important role. One may even use up to one full clock time to dump the charge on the floating-diffusion detector.

From a subjective point of view one can benefit from the triangular shape of the noise spectrum; given an equal objective noise performance the resistive feedback mode will be viewed as much better in noise performance.

It is shown that the resistive feedback mode can be made equal and/or better in signal-to-noise performance than a resetting floating-diffusion detector followed by the optimal signal processor.

REFERENCES

[1]) W.F. Kosonocky, J.E. Carnes, Charge-coupled digital circuits, IEEE J. Solid-State Circuits, **SC – 6** (5), 314–326 (1971).

[2]) J.E. Carnes, W.F. Kosonocky, Noise sources in charge-coupled devices, RCA Rev. **33**, 327–343 (1972).

[3]) E. Roks et. al. Theory and modeling of the floating-surface detector: an enhanced CCD output structure. Philips J. Res., **48**, 233 (1994).

[4]) P.G.M. Centen, personal communications.

[5]) P.G.M. Centen, CCD on-chip amplifiers: noise performance versus MOS transistor dimensions, IEEE Trans. Electron Devices, **ED – 38** (5) 1206–1216 (1991).

[6]) H.W. Wey and W. Guggenbühl, An improved correlated double sampling circuit for low noise charge-coupled devices, IEEE Trans. Circuits Syst., **37** (12) 1559–1565 (1990).

[7]) M.F. Tompsett and E.J. Zimany, Use of charge-coupled devices for delaying analog signals, IEEE J. Solid-State Circuits, **SC – 8** (2) (1973).

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