A 2/3-inch Low Noise HDTV FT CCD-Imager for 1080i180, 1080p90 and 720p120 Scanning at Constant Image Diagonal

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Acknowledgement

- DALSA Professional Imaging Eindhoven: Cees Draijer, Agnes Kleinmann, Jan Nooijen, Rene Leenen and Patrick van Gestel.
- Thomson Grass Valley Breda: Gerard van Beijsterveld, Paul Konings and Ruud van Ree.
- The sensor was developed as part of a MEDEA+ project (2A206) lead by Albert Theuwissen.

Agenda

- **Introduction**

- **4320 an important number**
  - Constant Image Diagonal
  - Scanning formats

- **Local oxide thinning**
  - Capacitance
  - Increase bandwidth
  - Reduce noise

Introduction: My World

In cooperation with DALSA we added functionality to the CCD-imager, that was not found in imagers of the competition.

HD-DPM gave a competitive edge

Super slow motion: 3x

Introduction

- **The HDTV standard……………………..**
  - 18 possible scanning formats
  - Main 1080p, 1080i and 720p…counted vertically
    - P:progressive; i:interlaced
  - The problem: to have ONE camera that supports 1080p, 1080i, 720p same horizontal angle of view.
  - In High end **2/3”,** Pro-AV ½” and 1/3”
    - Lens determined
- **1080p30 and 1080i60 and 720p60**
  - 74 MHz masterclock and 30 MHz video bandwidth
- **Triple speed**
  - 3x, sports applications (Olympics, soccer)
  - 1080p90 and 1080i180 and 720p180
  - 222 MHz masterclock and 90 MHz video bandwidth

The importance of

4320

pixels per column

Mathematics to arrive at the sweet spot

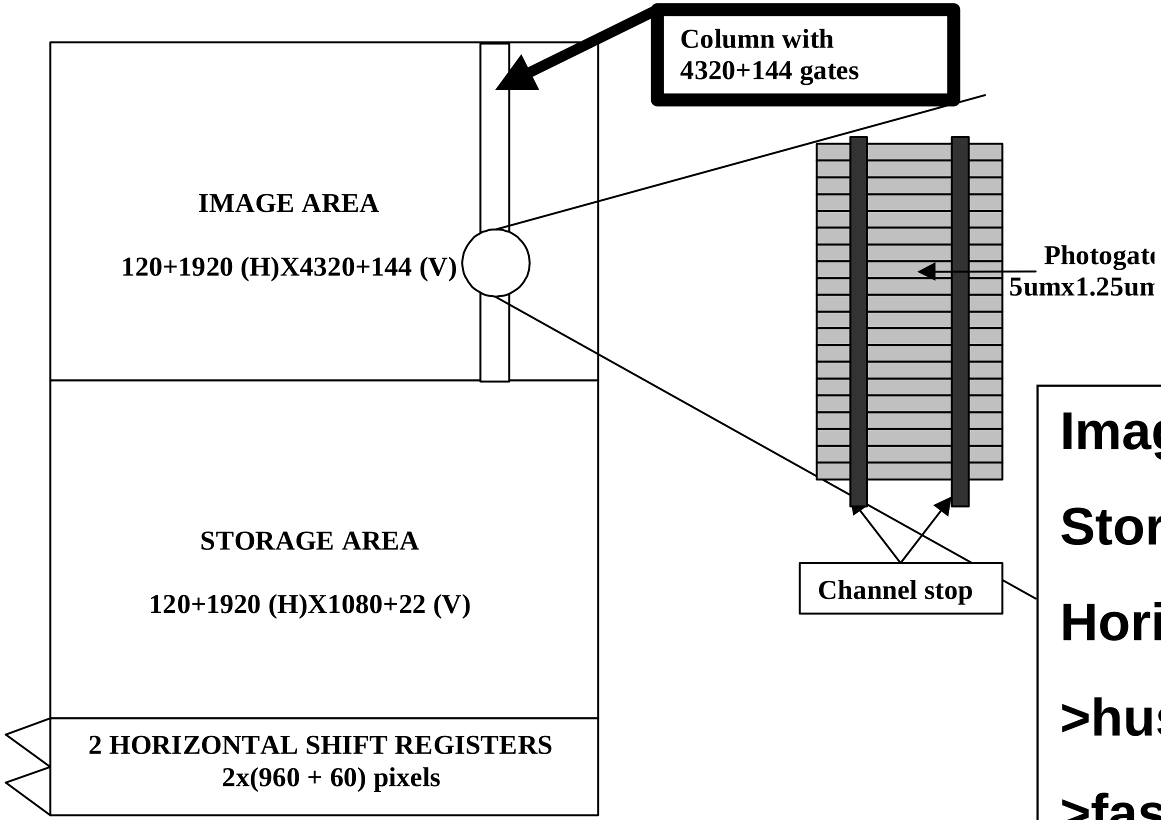
Scanning Format	Prime decomposition	Log-prime notation
1080P	$2^3.3^3.5$	[3,3,1,0,0,0]LP6
1080I	$2^2.3^3.5$	[2,3,1,0,0,0]LP6
720P	$2^4.3^2.5$	[4,2,1,0,0,0]LP6
480P	$2^5.3.5$	[5,1,1,0,0,0]LP6
480I	$2^4.3.5$	[4,1,1,0,0,0]LP6

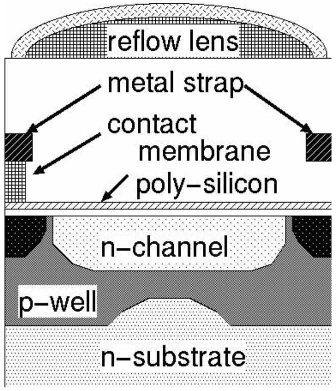
Least Common Multiple : $2^5 . 3^3 . 5 = 4320$

Constant Image Diagonal 1/3

=>SAME ANGLE OF VIEW for all scanning formats

=>1920 (H) x 4320 (V) and 16:9 aspect ratio
2/3" => 5 um x 1.25 um per photogate





Pixel cross-section

Imager area: 12-phase (9MHz)

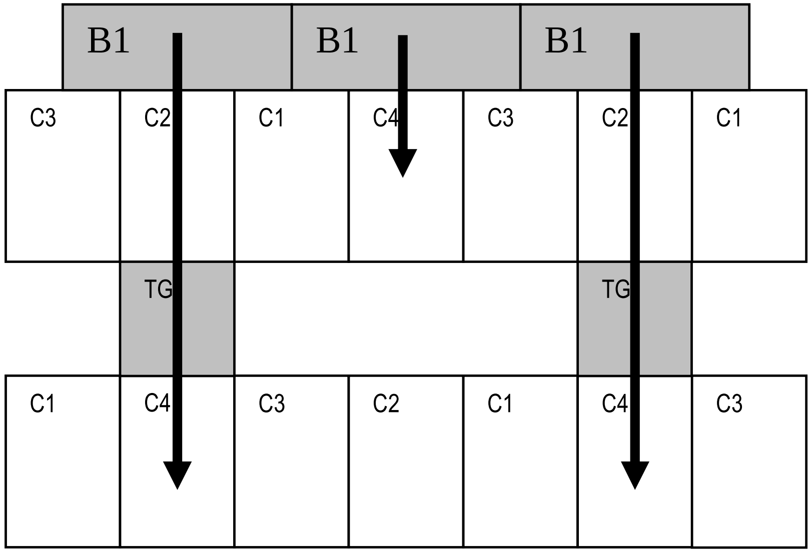
Storage area: 4-phase (9MHz)

Horizontal register: 4-phase

>hustle 4 independent voltages

>fast quasi 2-phase transport (2x111MHz)

Close up storage horizontal register



TOP-Register

BOTTOM-Register

pixels perfect aligned in time

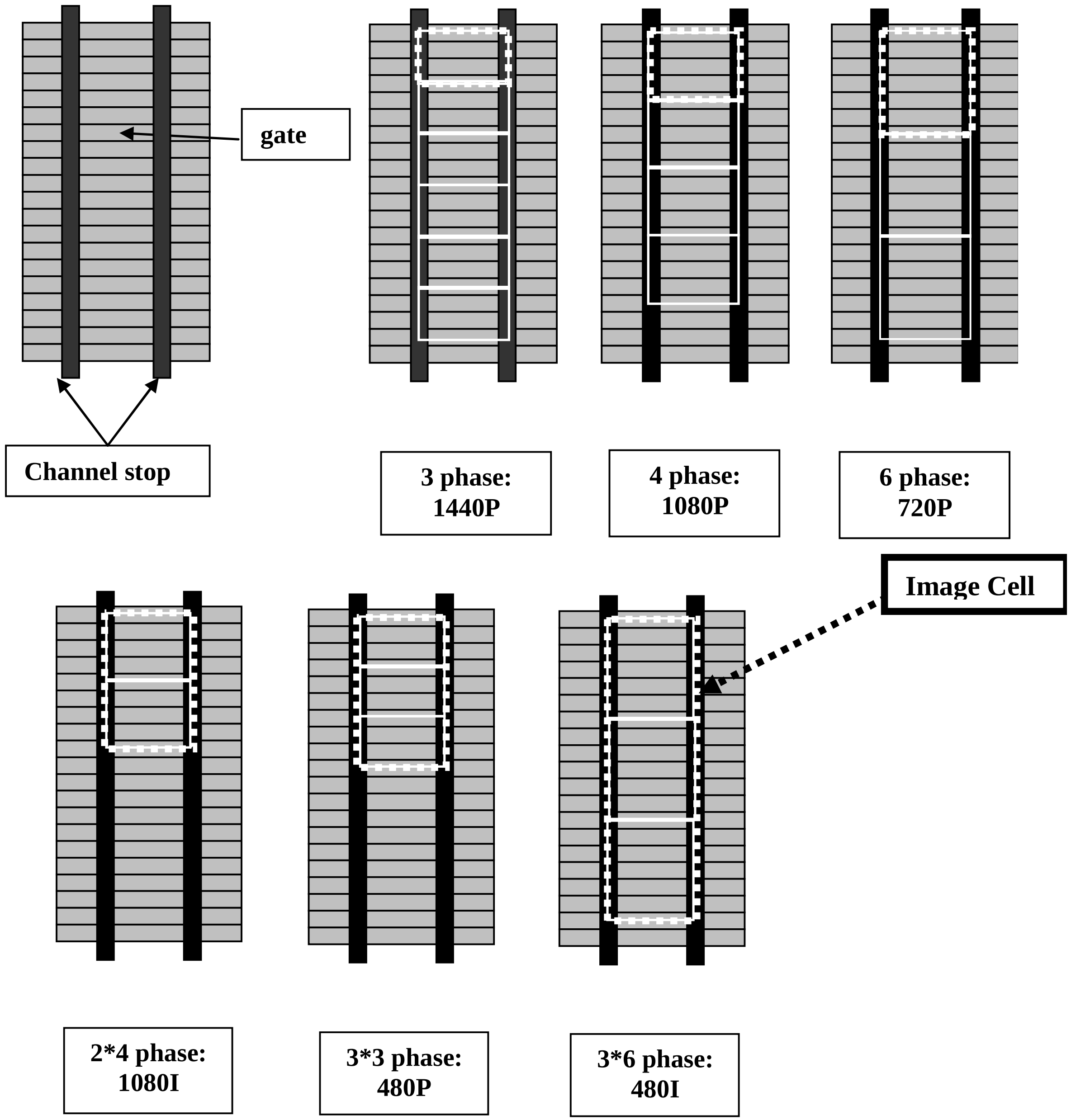
Constant Image Diagonal 2/3

- **What it is *designed* to do versus what it *can* do**

16:9 scanning formats	**#GATES/Pixel**	**In 12-phase clocking schema**
1080p	4 (= 4320 / 1080)	4-phase clocking 1 pixel
720p	6 (= 4320 / 720)	6-phase clocking 1 pixel
1080i	8 (= 4320 / (1080/2))	4-phase clocking 2 sub-pixels
480p	9 (= 4320 / 480)	3-phase clocking 3 sub-pixels
576i	15 (= 4320 / (576/2))	3-phase clocking 5 sub-pixels
480i	18 (= 4320 / (480/2))	6-phase clocking 3 sub-pixels
1080p in 2.37:1 aspect ratio	3 (= 4320*(3/4) / 1080)	3-phase clocking 1 pixel

=>2.37:1 is used for cinemascope

Constant Image Diagonal 3/3

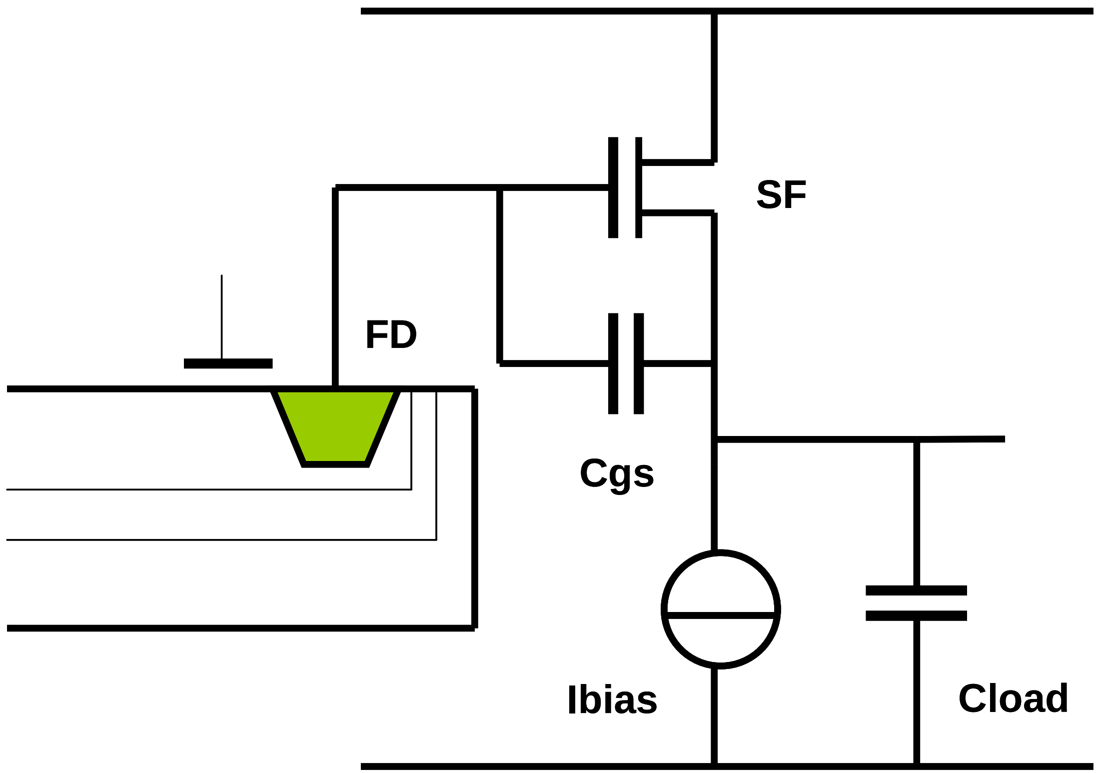


2/3” => HxV
5 um x 1.25 um
per photogate

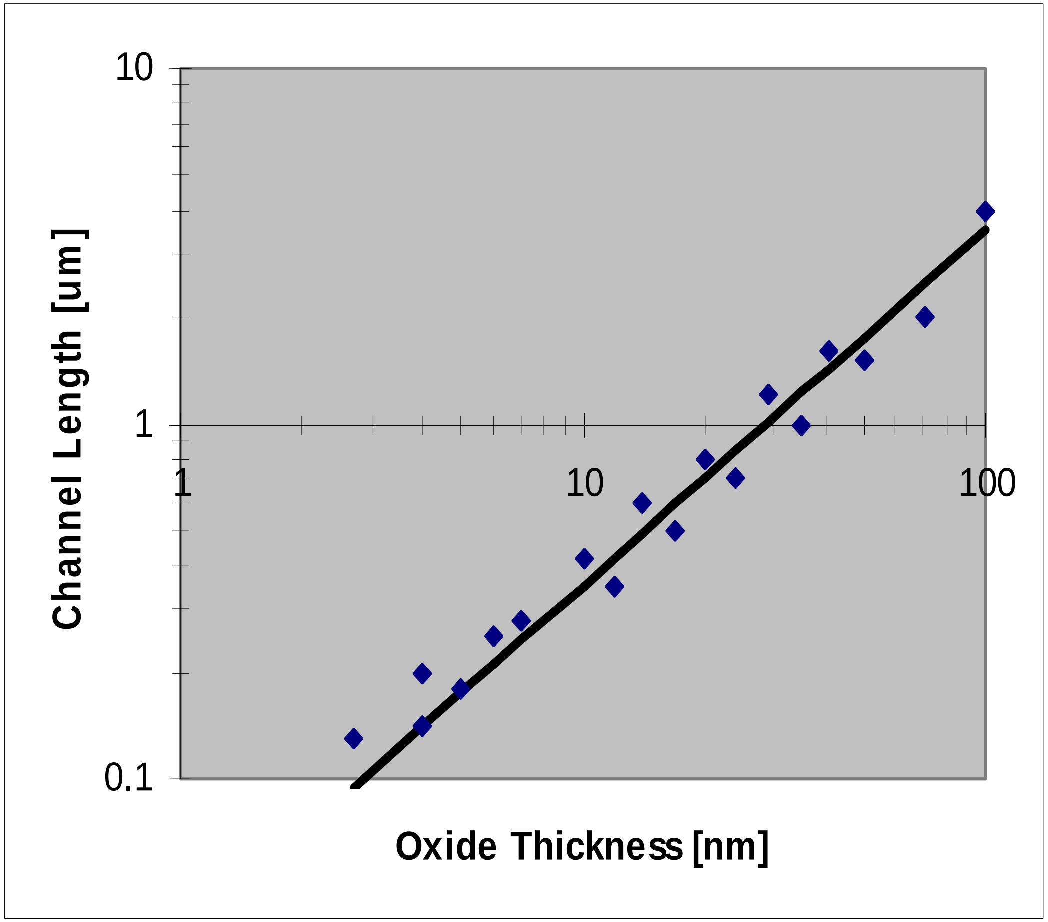
Noise and bandwidth

High bandwidth low noise

- **Using local oxide thinning for the MOST to optimize noise and bandwidth performance**
  - “Pixel” oxide thickness determines CCD performance decouple it!



Channel Length and Oxide Thickness



Minimum channel length

$$L_{\min} \approx 35 * d_{ox}$$

Based on Wong's data (IEEE ED 1996)

(equal units)

MOST Gate capacitance scaling

$$C_g = W * L * C_{ox} = W * L * \frac{\varepsilon}{d_{ox}}$$

- **Based on Wong's data (equal units)**

$$L_{\min} \approx 35 * d_{ox}$$

- **The gate capacitance only proportional to W**

$$\boxed{C_g \approx W}$$

Bandwidth

- **Given a load capacitance and MOST transconductance the 3dB frequency is**

$$F_{3dB} = \frac{g_m}{2 * \pi * C_{load}}$$

$$I_{ds} = W * J_x$$

$$\boxed{g_m = \sqrt{2 * \frac{W}{L} * \frac{\varepsilon}{d_{ox}} * u_n * I_{ds}} \approx \frac{W}{d_{ox}} \approx \frac{1}{d_{ox}}}$$

Halving the oxide thickness and channel length doubles the bandwidth.

While having same input capacitance Cg ….important for 3-stage amp

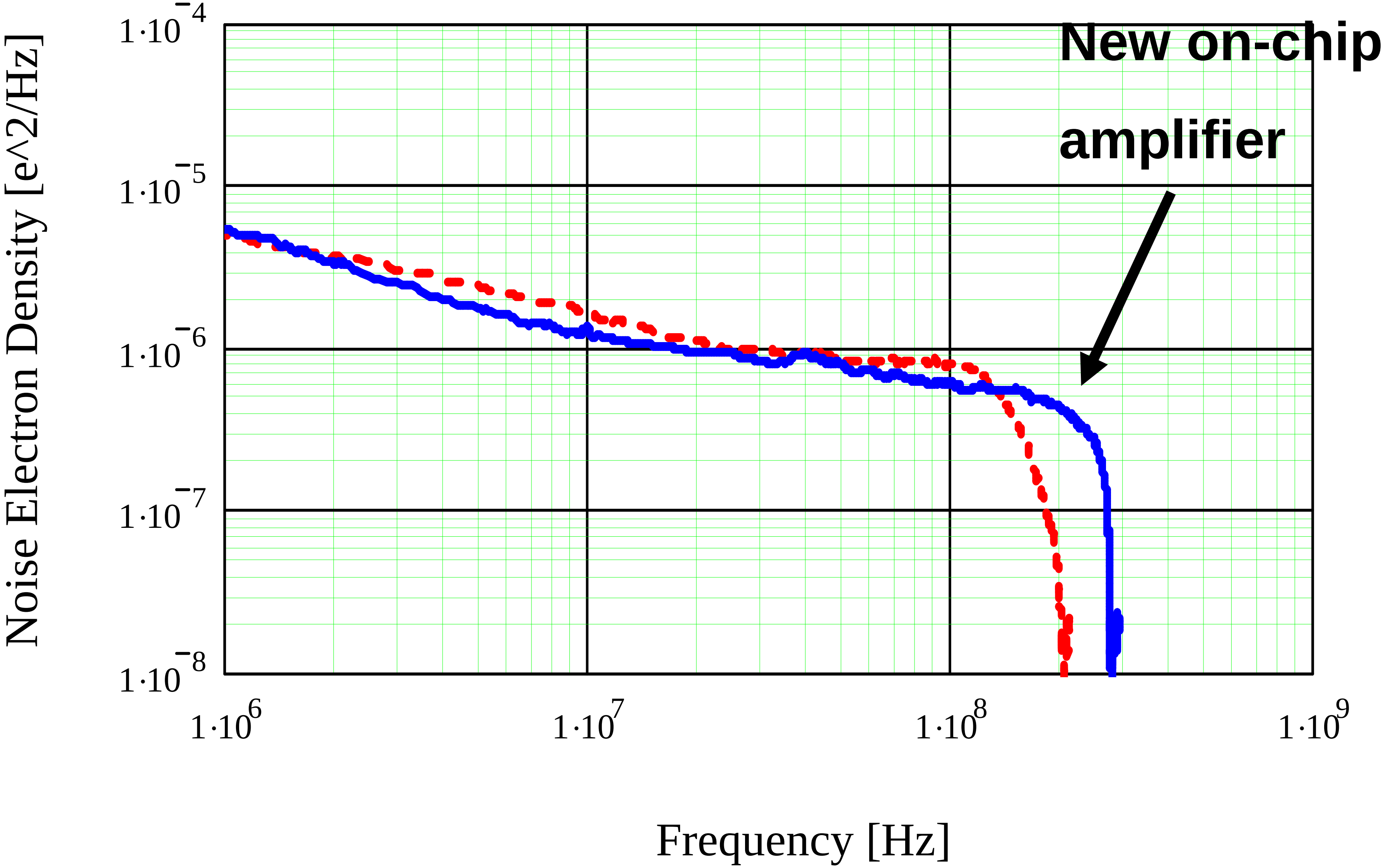
Noise

$$NED = \frac{4kT}{g_m} * \left(\frac{C_{tot}}{q} \right)^2$$

– Optimal gate capacitance approx. the MOST dimensions independent capacitance, and thus a given
– Minimizing the noise electron density…only gm left.
– But W is fixed…..capacitance determined

$$g_m = \sqrt{2 * \frac{W}{L} * \frac{\varepsilon}{d_{ox}} * u_n * I_{ds}} \approx \frac{W}{d_{ox}} \approx \frac{1}{d_{ox}}$$

Noise Spectrum……a first result



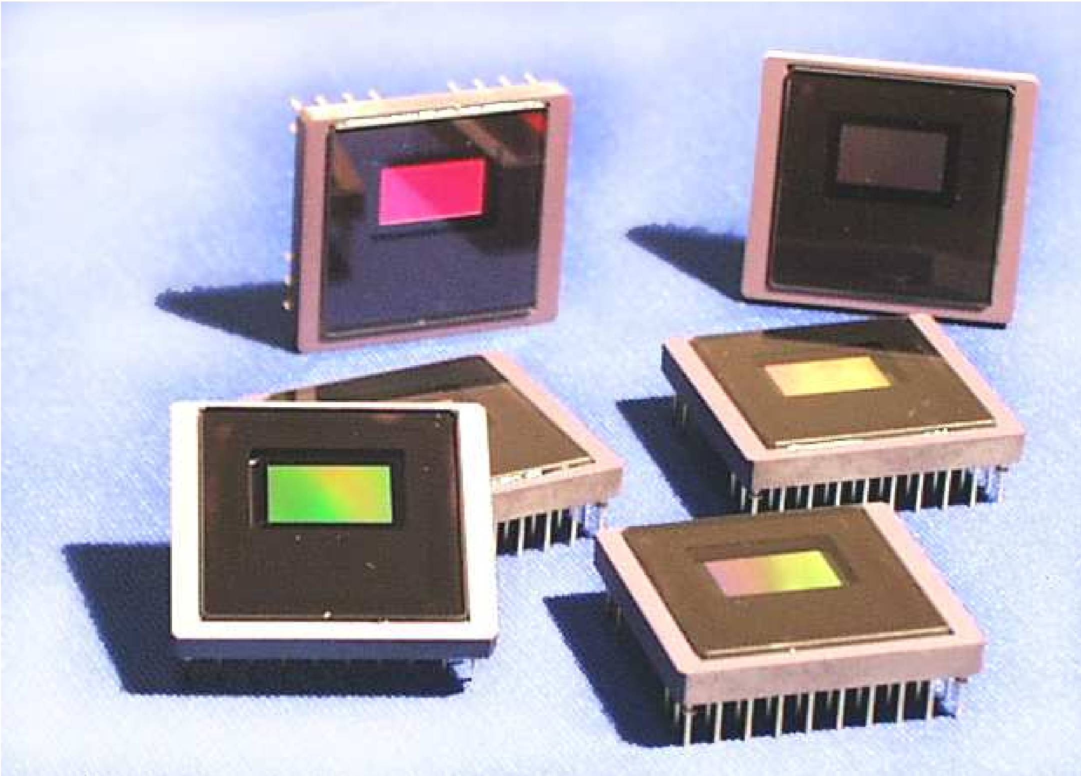
Benchmarking

Type	Ref	Reset Frequency	Ampl. Type	Conversion gain	Noise after CDS/ √Resetfrequency
FF-CCD	ED1997 Burke	100 kHz	Source Follower	20 µV/e	6.3 e/√MHz
CMOS	AIS2003 Krymski	50 kHz	Source Follower +Gain	60 µV/e	6.3 e/√MHz
FF-CCD	AIS2005 Draijer	25 MHz	Source Follower	40 µV/e	2.8 e/√MHz
CMOS	ISSCC2005 Kozlowski	104 kHz	Source Follower +Gain	?µV/e	46 e/√MHz
CMOS	ISSCC2006 Yoshihara	156 kHz	Source Follower +Gain	40 µV/e	17.7 e/√MHz
CMOS	ISSCC2007 Takahashi	156 kHz	Source Follower +Gain	75 µV/e	11.6 e/√MHz
CMOS	ISSCC2007 Cho	625 kHz	Source Follower +Gain	101 µV/e	10.4 e/√MHz
FT-CCD	This paper	111MHz	Source Follower	18 µV/e	1.3 e/√MHz

Table

Technology	Tungsten, thin transparent membrane Frame Transfer CCD		Number of horizontal registers	2
Chip Size	12.0(H) x 12.7(V) mm^2		Number of horizontal clock phases During fast horizontal transport	4 Quasi 2-phase operation
Aspect Ratio	16:9		Number of on-chip amplifiers	2
Storage number of clock phases	4		Measured bandwidth of on-chip amplifier	>241MHz
Storage number of columns x lines	2040(H) x 1102(V)		Conversion gain	18 µV /e
Image number of clock phases	12		Max frame rate, pixel rate	180 fld/sec, 223Mpixel/sec
Image number of columnsxgates	2040(H) x 4464(V)		Horizontal transport frequency	2x112MHz
Pixel size in 1920x1080p90	5.0 µm x 5.0 µm (HxV)		Vertical transport frequency	10MHz
Pixel size in 1920x1080i180	5.0 µm x 5.0 µm x 2 (HxV)		Noise Electron Density (NED) of the on-chip amplifier	0.75 e^2/MHz@37.125MHz 0.59 e^2/MHz@112MHz
Pixel size in 1920x720p120	5.0 µm x 7.5 µm (HxV)		Temporal Noise After CDS in 30MHz	8e or 2.1 e^2/MHz
Pixel size in 1920x1080p90 @ 2.37:1	5.0 µm x 3.75 µm (HxV)		Sensitivity in Green	820 electrons/lux/sec/μm^2
			Qmax	680 electrons/μm^2

HD-DPM Imager



Conclusion

- **A 2/3” multi-format HDTV imager was developed**
  - With equal angle of view in 1080p, 1080i and 720p
  - Running at 1920x1080i180
  - 180 fields/second
  - Horizontal transport at 2x111MHz
  - Vertical transport at 9.25MHz

- **Low noise (0.59 e^2/MHz@111MHz) and high bandwidth (>240MHz) can be reached simultaneously when use is made of local oxide thinning as an additional optimization parameter for MOS transistors in the on-chip amplifier**

- **The triple speed HDTV camera, applying this imager, was used during the 2008 Olympics in Beijing and the 2008 European soccer games**

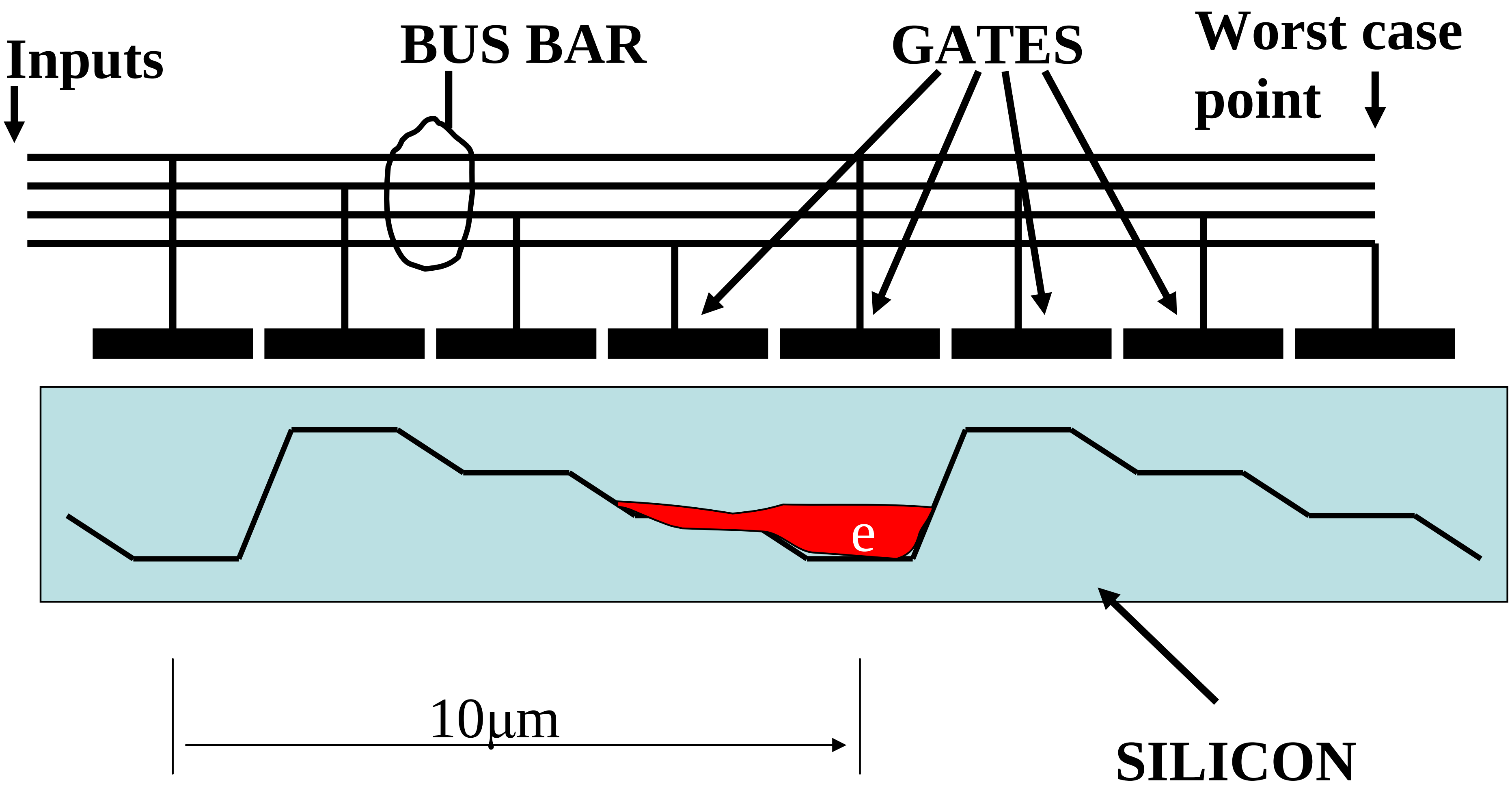
Q&A

Bonus material

An analytical approach

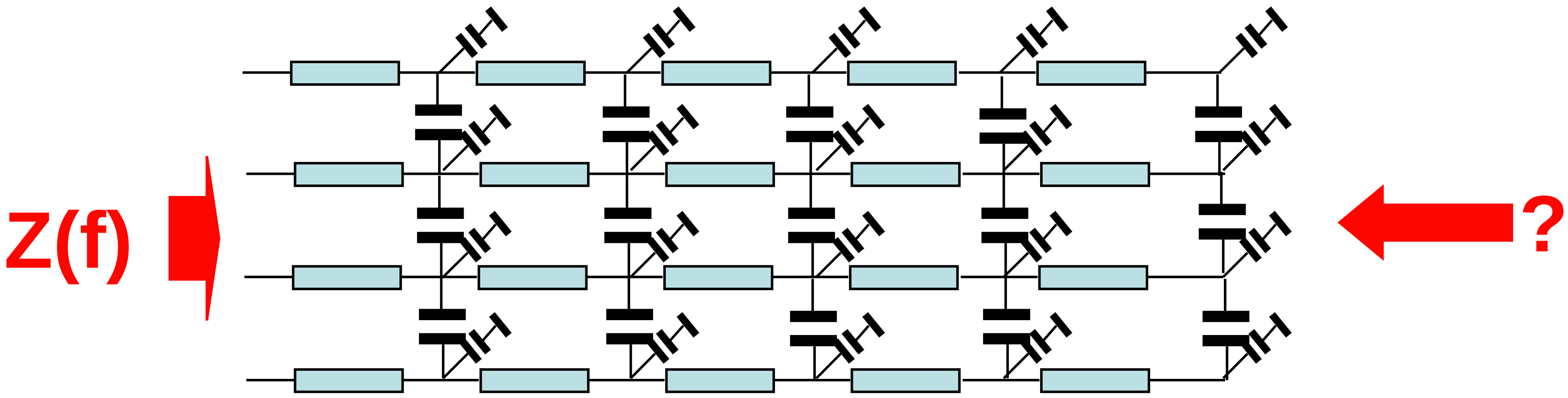
for the imager internal clock distribution

CCD charge transport



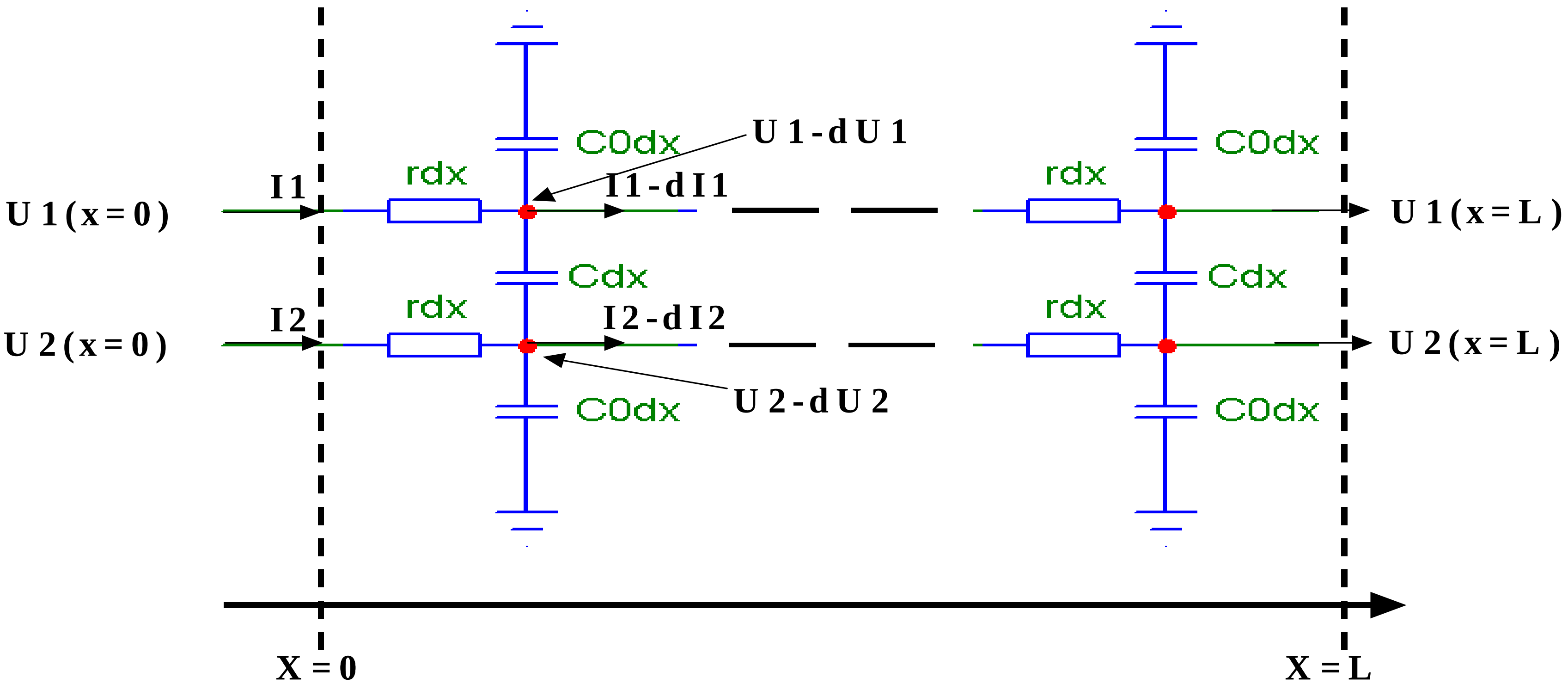
The general question

- **Use the fact that a lumped model with over 4000 discrete elements can be approximated very well with a few coupled partial differential equation**



- **Solving them resulted in a closed form equation with the series resistance, parallel capacitance per unit length, cross capacitance and length of transportregister as a parameter.**

Quasi 2-phase



The equations

Measurable

$$Z(f) := \frac{2 \cdot r}{\lambda(f) \cdot \tanh(\lambda(f) \cdot L) + \mu(f) \cdot \tanh(\mu(f) \cdot L)}$$

$$H(f) := \frac{U(L, f)}{U(0, f)}$$

Predictable

$$H(f) := e^{-\lambda(f) \cdot L} \cdot (1 + \tanh(\lambda(f) \cdot L))$$

SOLUTION

$$\frac{d}{dx} U(L, t) := 0 \qquad U(0, t) := V$$

$$\lambda(f) := \sqrt{1j \cdot 2 \cdot \pi \cdot f \cdot r \cdot (C0 + 2 \cdot C)}$$

$$\mu(f) := \sqrt{1j \cdot 2 \cdot \pi \cdot f \cdot r \cdot C0}$$

BOUNDARY CONDITIONS

PARAMETERS

$$\frac{d}{dx}\frac{d}{dx} I(x, t) := (C0 + 2 \cdot C) \cdot r \cdot \frac{d}{dt} I(x, t)$$

$$\frac{d}{dx}\frac{d}{dx} U(x, t) := (C0 + 2 \cdot C) \cdot r \cdot \frac{d}{dt} U(x, t)$$

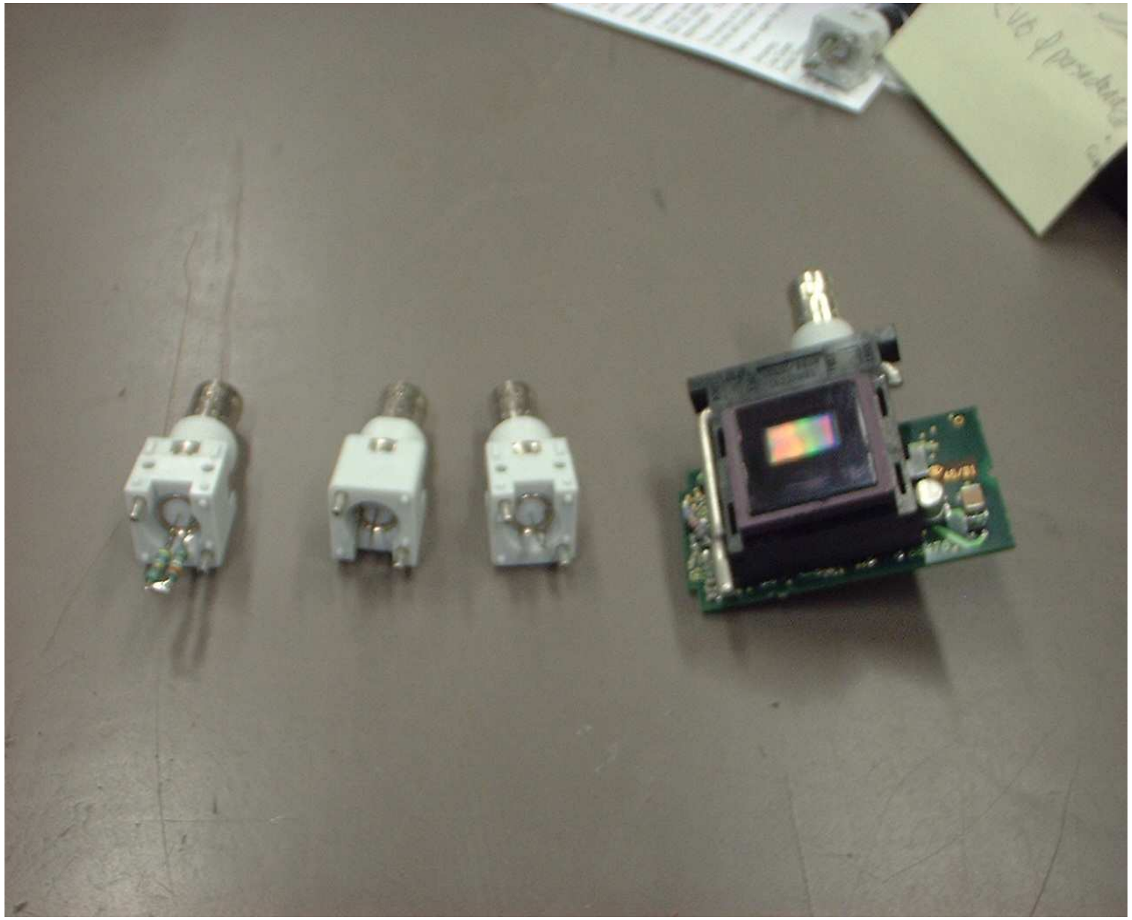
DIFFERENTIATION and SUBSTITUTION

$$\frac{d}{dx} I(x, t) := (C0 + 2 \cdot C) \cdot \frac{d}{dt} U(x, t)$$

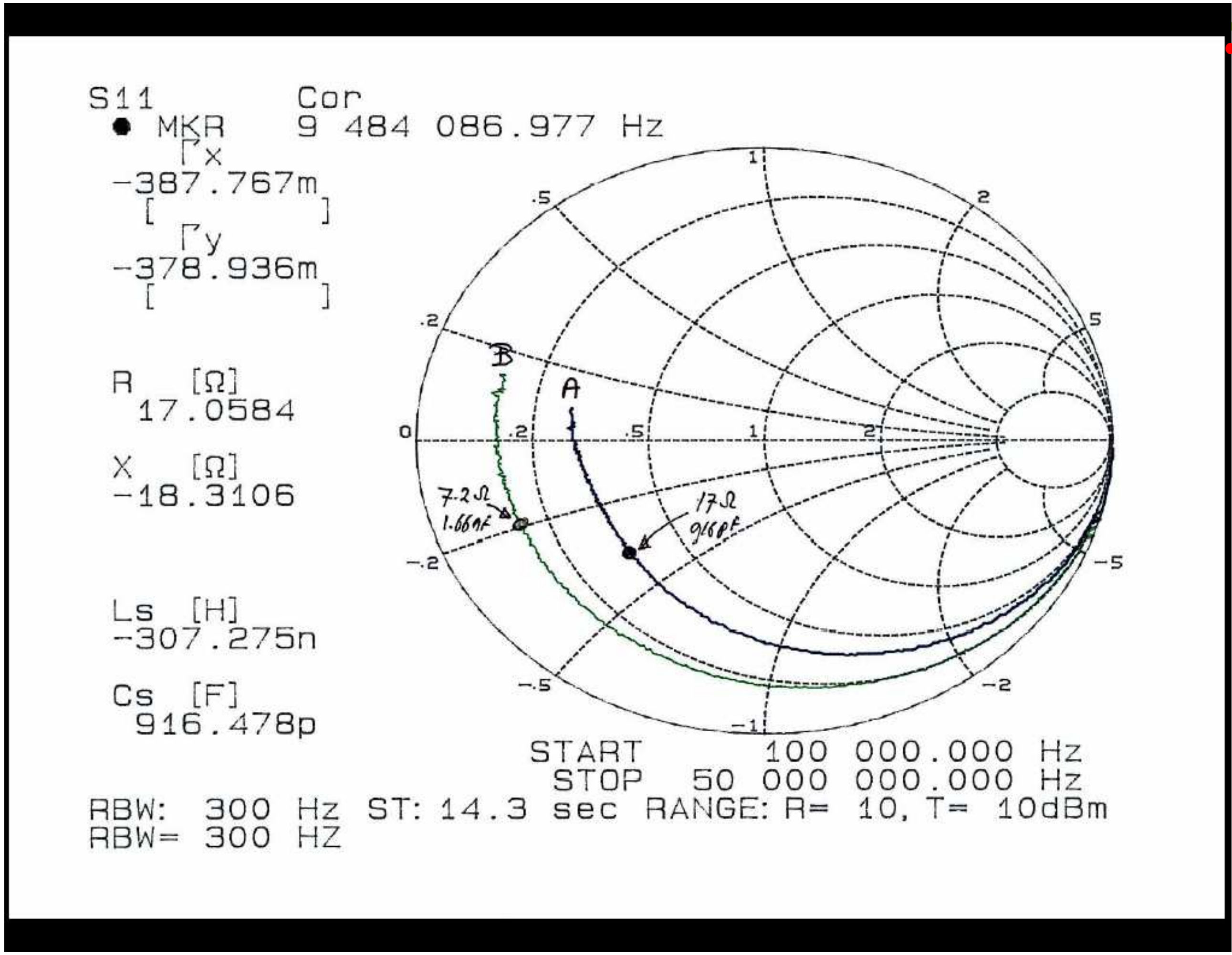
$$\frac{d}{dx} U(x, t) := r \cdot I(x, t)$$

The measurement

- Calibration of the network-analyser reflectometer setup
  - **3 kind of terminators needed**
    - **Open**
    - **Short**
    - **Characteristic impedance**
- Measure the parameters on the PCB with imager

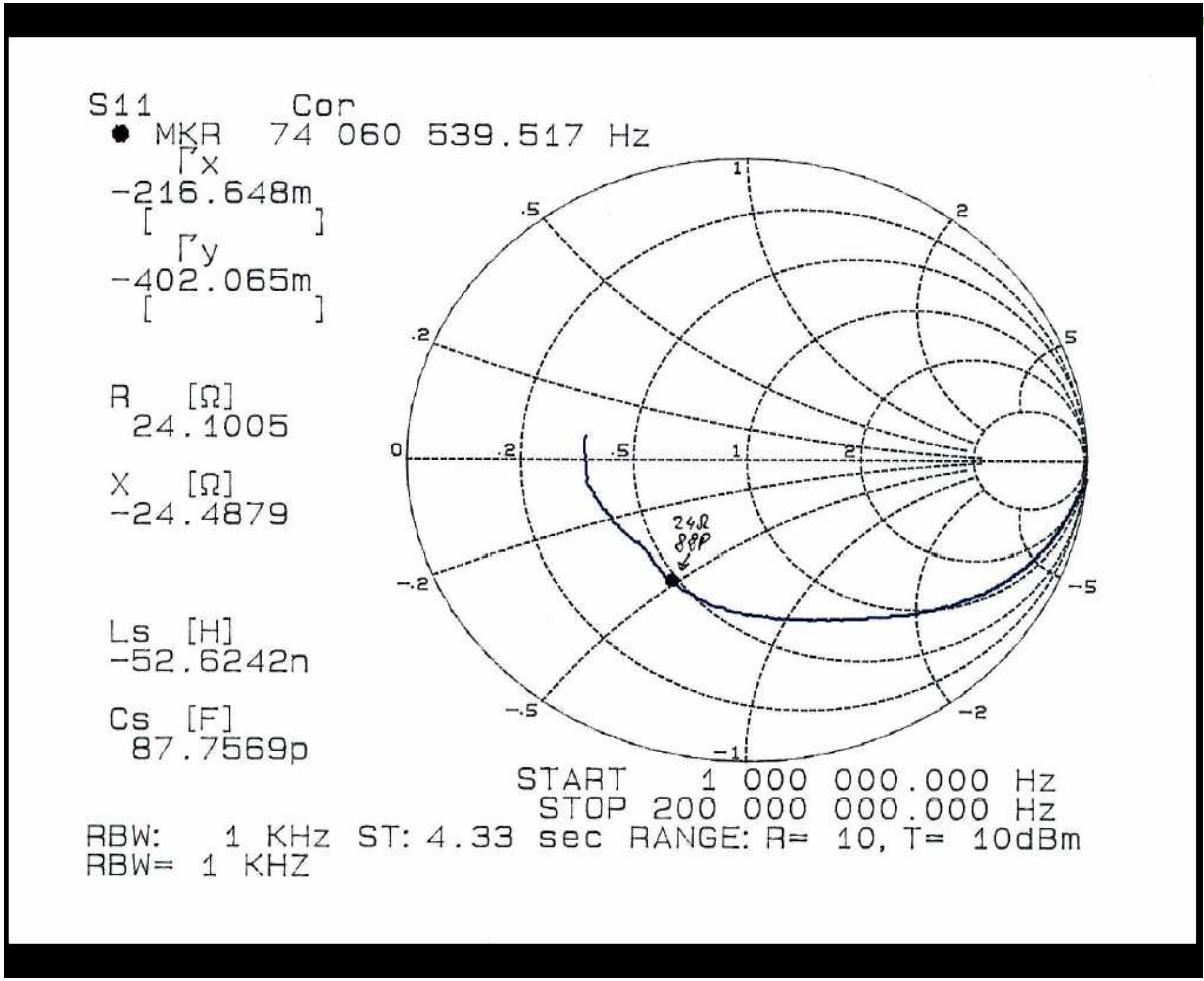


Smith-chart of vertical phases



- **Input impedance of the Image and Storage clock lines**
  - Horizontal axis is the real part of the impedance the vertical axis the imaginary part.
  - The impedance crosses the real axis at some point showing that there is also some self-inductance in the circuit.
  - Marker at 9.48MHz and is close to the 2-speed VTR.
  - The series R and C at that frequency are:
    - 17 Ohm and 916 pF for the image clock and
    - 7.2 Ohm and 1.66nF for the storage clock.

Smith-chart of horizontal phases



- **Impedance of the horizontal clock lines**
  - Driven in quasi 2-phase.
  - The frequency sweeps from 1 MHz to 200 MHz.
  - At 74 MHz, near the driving frequency of 2-speed mode, the equivalent series resistance is 24 Ohm and capacitance is 88 pF.